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I D E N T I F I C A T I O N

PRODUCT CODE: AC-T437A-MC

PRODUCT NAME: CNDUQA0 DUV11 OFLNE LGC TSTS

PRODUCT DATE: DEC , 1982

MAINTAINER: DIAGNOSTIC SERVICES/ISS

AUTHOR: J.CARMODY

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GENERAL DESCRIPTION

THIS DIAGNOSTIC CAN CHAIN 16 DUV11'S. THIS MEANS THAT 16 DEVICES CAN BE SEQUENTIALLY EXERCISED. THE DIAGNOSTIC MAKES ONE PASS BEFORE PROCEEDING TO THE NEXT DEVICE, AND CONTINUES EXERCISING ALL DEVICES IN THIS FASHION UNTIL HALTED.

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- 1. THE DUV11 OFFLINE LOGIC TESTS VERIFY THAT ALL REGISTERS EXIST AND ALL RESPECTIVE BITS CAN BE MASTER CLEARED, READ, WRITTEN AND/OR READ/WRITTEN

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2. REQUIREMENTS

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PDP-11/21 COMPUTER (LSI)

DUV11 SYNCHRONOUS/ISOCRONOUS OPTION

ONE CONSOLE TELETYPE OR EQUIVALENT

2.2 STORAGE

THE PROGRAM LOADS INTO 4K OF MEMORY WITH BOOTSTRAP

3. LOADING PROCEDURE

THE STANDARD PROCEDURE FOR LOADING ABSOLUTE BINARY TAPES IS TO BE USED.

STARTING ADDRESS
FOR ABSOLUTE LOADER

4K	017500
8K	037500
12K	057500
16K	077500
20K	117500
24K	137500
28K	157500

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

NOTE: ALL SWITCHES RESIDE INTERNAL TO THE CPU AT ADDRESS 176. THESE MAY BE SET VIA THE CONSOLE TTY BY DIRECTLY MODIFYING LOC. 176.

NOTE: RUNNING UNDER APT-11, THERE IS A USER SWITCH REGISTER CALLED '\$USWR'. IN ORDER TO BE FLEXIBLE ON THE AVAILABILITY OF THE H315 CONNECTOR, ONE BIT PASSES STATUS TO APT-11. BIT 0 IN \$USWR REFLECTS THIS STATUS, A 0 = CONNECTOR PRESENT, A 1 = CONNECTOR NOT AVAILBLE.

THE USER CHANGES THE CONTENTS OF THIS LOCATION
WHEN BUILDING THE E TABLE, BY ANSWERING THE
PROMPT "SWITCH 2".

- 4.1.1 AFTER PROGRAM LOAD (INITIAL PROGRAM START)
ALL CONSOLE SWITCHES DOWN
- 4.1.2 TO MODIFY DEVICE VECTOR AND CONTROL REGISTER ADDRESSES
AFTER PROGRAM RESTART OR TO RUN MULTIPLE DEVICES
SW00=1
- 4.1.3 TO START PROGRAM AT SELECTED TEST AFTER A PROGRAM RESTART
(ONLY IN SINGLE DEVICE TESTS)
SW01=1
- 4.1.4 TO LOCK ON SELECTED TEST AFTER A PROGRAM RESTART
(ONLY IN SINGLE DEVICE TESTS)
SW14=1
NOTE1: IN GENERAL SW01 WILL BE USED WHEN SW14=1 IS USED
NOTE2: WITHOUT SW01=1 "LOCK ON TEST" WILL DEFAULT TO TEST 1
- 4.2 STARTING ADDRESS
THE STARTING ADDRESS FOR ALL TESTS IS 000200
THE STARTING ADDRESS FOR ALL TESTS IS 000200
THE STARTING ADDRESS TO ENTER A SELECTED TEST IS 000200
THE STARTING ADDRESS TO LOCK ON TEST IS 000200
- 4.3 PROGRAM AND/OR OPERATOR ACTION
 - 4.3.1 INITIAL PROGRAM START
 - 4.3.1.1 LOAD PROGRAM INTO MEMORY WITH ABSOLUTE LOADER
 - 4.3.1.2 SET SWITCH REGISTER (LOC. 176) TO ZERO.
 - 4.3.1.3 TYPE 200G.
 - 4.3.1.4 PROGRAM WILL START.
 - 4.3.1.5 THE PROGRAM WILL TYPE 'DUV11 CZDUQ-C TAPE A' (ONCE ONLY)
 - ★ .REM ★
 - ★
 - ★ .REM ★
 - 4.3.1.6 THE PROGRAM WILL TYPE 'R' TO INDICATE THAT IT IS ABOUT
TO START TESTING ,AND THEN TESTING WILL BEGIN
 - 4.3.2 PROGRAM RESTART WITH ALL SWITCHES DOWN
 - 4.3.2.1 THE PROGRAM WILL TYPE 'R' AND WILL COMMENCE TESTING
 - 4.3.3 PROGRAM RESTART WITH SW00=1

- 4.3.3.1 SET SWITCH REGISTER (LOC. 176) TO A 000001.
- 4.3.3.2 TYPE 200G.
- 4.3.3.3 PROGRAM WILL START.
- 4.3.3.4 THE PROGRAM WILL TYPE " 1ST DEVICE: RECEIVER CONTROL REGISTER ADDRESS" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD
- 4.3.3.5 TYPE IN THE ADDRESS OF THE FIRST RECEIVER CONTROL REGISTER ADDRESS OF THE DUV11 TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.4

- 4.3.3.6 THE PROGRAM WILL TYPE "VECTOR ADDRESS-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD
- 4.3.3.7 TYPE IN THE BASE RECEIVER INTERRUPT VECTOR ADDRESS FOR THE DUV11 TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.6

- 4.3.3.8 THE PROGRAM WILL TYPE "ARE YOU RUNNING MULTIPLE DEVICES ?" (Y OR N)-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD
- 4.3.3.9 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ANSWER IS GIVEN, THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.8

IF A 'NO' ANSWER IS GIVEN: JUMP TO SECTION 4.3.3.12
IF A 'YES' ANSWER IS GIVEN:THE NEXT QUESTION IS ASKED

- 4.3.3.10 THE PROGRAM WILL TYPE "LAST DEVICE:RECEIVER CONTROL REGISTER ADDRESS-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD
- 4.3.3.11 TYPE IN THE ADDRESS OF THE LAST RECEIVER CONTROL REGISTER ADDRESS OF THE DUV11 TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.10
NOTE:ALL ADDRESSES SHALL BE CONTIGUOUS

- 4.3.3.11.1 IF AN 'OUT OF RANGE' ADDRESS IS TYPED IE. MORE THAN 16 (10) DEVICES AWAY (UPWARDS).....THE PROGRAM WILL TYPE 'OUT OF RANGE:RETYPE LAST DEVICE RXCSR ADDRESS-'

AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.11.2 TYPE IN THE ADDRESS OF THE LAST RECEIVER CONTROL REGISTER ADDRESS OF THE DUV11 TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL REPEAT THE MESSAGE OF 4.3.3.11.1

IF A DEVICE ADDRESS LOWER THAN 1ST DEVICE ADDRESS IS TYPED.....
.....SCHOOLS OUT.....THERE IS NO PROTECTION FOR THIS.
THE PROGRAM WILL DEFAULT TO TWO DEVICES ACTIVE (UPWARDS FROM 1ST DEVICE ADDRESS).THE SAME APPLIES TO IDENTICAL ADDRESSES TYPED FOR FIRST AND LAST DEVICE.
OBSERVE LOCATION @ ACTREG: SEE SECTION 7.2

4.3.3.12 THE PROGRAM WILL TYPE "# OF SYNC CHARS SELECTED (1 OR 2)-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD. REFER TO MANUAL FOR PROPER SWITCH SETTINGS OF SWITCH E55-4.

4.3.3.13 TYPE IN THE APPROPRIATE ANSWER "1" OR "2" FOLLOWED BY A <CARRIAGE RETURN>.(NOTE:ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL REPEAT THE MESSAGE OF 4.3.3.12

4.3.3.14 THE PROGRAM WILL TYPE " IS SEC XMIT SWITCH E55-2 ON? (Y OR N)-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.15 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY A <CARRIAGE RETURN>.(NOTE THAT ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL REPEAT THE MESSAGE OF 4.3.3.14

4.3.3.16 THE PROGRAM WILL TYPE "IS SEC REC SWITCH E55-3 ON? (Y OR N)-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.17 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY A <CARRIAGE RETURN>. (NOTE: ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL REPEAT THE MESSAGE OF 4.3.3.16

4.3.3.18 THE PROGRAM WILL TYPE "IS OPT CLR ENABLE SWITCH E55-1 ON? (Y OR N)-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.19 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED

BY A <CARRIAGE RETURN>. (NOTE: ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL REPEAT THE MESSAGE OF 4.3.3.18

4.3.3.20 THE PROGRAM WILL TYPE "ARE YOU RUNNING IN MAINT.
MODE EXTERNAL ? ANDDO YOU HAVE THE EXTERNAL MODEM
BYPASS JUMPER CONNECTOR ON ? (Y OR N)-" AND WAIT FOR AN
INPUT FROM THE TELETYPE KEYBOARD

4.3.3.21 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY
A <CARRIAGE RETURN>. (NOTE: ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL REPEAT THE MESSAGE OF 4.3.3.20

4.3.3.22 THE PROGRAM WILL TYPE 'R' TO INDICATE THAT IT
HAS STARTED AND WILL COMMENCE TESTING AT TEST 1

4.3.4 PROGRAM RESTART WITH SW01=1
NOTE: THIS WILL ONLY WORK WHEN A SINGLE DEVICE IS SELECTED
...IT WILL NOT WORK IF MULTIPLE DEVICES ARE SELECTED

IF MULTIPLE DEVICES WERE PREVIOUSLY SELECTED,LOAD 000200,
AND SELECT SW00=1 AND ANSWER 'NO' TO THE MULTIPLE DEVICE QUESTION
SEE 4.3.3

4.3.4.1 SET SW01=1 IN SWITCH REG (LOC. 176)

4.3.4.2 TYPE 200G.

4.3.4.3 PROGRAM WILL START.

4.3.4.4 THE PROGRAM WILL TYPE "TEST PC-" AND WAIT FOR AN INPUT FROM
THE TELETYPE KEYBOARD

4.3.4.5 TYPE IN THE ADDRESS OF THE TEST AT WHICH THE PROGRAM IS TO
BE STARTED FOLLOWED BY A <CARRIAGE RETURN>

4.3.4.6 THE PROGRAM WILL TYPE 'R' TO INDICATE THAT IT HAS STARTED
TESTING AT THE SELECTED TEST

NOTE: CARE MUST BE TAKEN WHEN THIS FEATURE IS USED
SINCE THERE IS NO PROTECTION AGAINST SELECTING AN ADDRESS
THAT IS IN THE MIDDLE OF A TEST

4.3.5 PROGRAM RESTART WITH SW14 =1
NOTE: THIS WILL ONLY WORK WHEN A SINGLE DEVICE IS SELECTED
SEE NOTE IN 4.3.4 FOR MORE DETAILS

4.3.5.1 SET SW14=1 IN SWITCH REG. (LOC. 176)

4.3.5.2 TYPE 200G.

4.3.5.3 PROGRAM WILL START.

4.3.5.4 THE PROGRAM WILL TYPE 'LOCK ON SELECTED TEST ? (Y OR N)-'
AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.5.5 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY A
<CARRIAGE RETURN>

IF A NO ANSWER IS GIVEN: THIS LOCK ON TEST WILL BE IGNORED
AND THE PROGRAM WILL TYPE 'R' TO INDICATE THAT IT HAS STARTED
TESTING AT TEST 1

4.3.5.6 IF A YES ANSWER WAS GIVEN:THE PROGRAM WILL ACT AS FOLLOWS...
THE PROGRAM WILL TYPE 'R' TO INDICATE THAT IT HAS STARTED
TESTING AT TEST 1 AND WILL REMAIN IN TEST 1 UNTIL HALTED
OR IF ANY KEY IS STRUCK ON THE TELETYPE ,THE PROGRAM
WILL FREEZE ON THE NEXT TEST UNTIL A KEY IS STRUCK ON
THE TELETYPE AND SO FORTH THRU THE PROGRAM. IF SW01 =1 IT
WILL PERFORM AS IN SECTION 4.3.4 ALLOWING ONE TO FREEZE
ON A SELECTED TEST RATHER THAN DEFAULTING TO TEST 1

5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS (INTERNAL TO THE CPU, ACCESSED VIA LOC. 176).

SW15 =1 HALT ON ERROR
SW14 =1 LOOP ON CURRENT TEST
SW13 =1 INHIBIT ERROR TYPEOUT
SW11 =1 INHIBIT ITERATIONS
SW10 =1 ESCAPE TO NEXT TEST ON ERROR
SW09 =1 LOOP ON ERROR
SW01 =1 RESTART PROGRAM AT SELECTED TEST
SW00 =1 RESELECT VECTOR AND CONTROL REGISTER ADDRESSES
&PARAMETERS AFTER A PROGRAM RESTART
TO INHIBIT 'END OF PASS' TYPEOUT - TURN TELETYPE OFF

6. ERRORS

6.1 ERROR HALTS (UNDER LSI ALL HALT ERRORS RETURN CONTROL TO O.D.T.)
THERE ARE FOUR DISTINCT ERROR TYPEOUTS

6.1.1 PC+2 = ERROR PC
WHERE PC +2 IS THE ADDRESS OF THE CALL TO THE ERROR HANDLER +2
REFER TO THE ABOVE 'HLT' IN DIAGNOSTIC FOR ERROR DESCRIPTION

CHECK ADDRESS @ RXCSR: TO LOCATE THE DEVICE PRESENTLY UNDER
TEST WHEN RUNNING MULTIPLE DEVICES

6.1.2 PC +2 = REGISTER ERROR PC
REGISTER EXPECTED ACTUAL
1XXXXX YYYYYY ZZZZZZ

WHERE 1XXXXX IS THE ADDRESS OF THE FAILING DEVICE REGISTER

WHERE YYYYYY IS THE EXPECTED CONTENTS OF THAT REGISTER

WHERE ZZZZZZ IS THE ACTUAL CONTENTS OF THAT REGISTER

6.1.3 PC +2 = RECEIVER ERROR PC
REGISTER EXPECTED ACTUAL
1XXXXX YYYYYY ZZZZZZ

WHERE 1XXXXX IS THE ADDRESS OF THE FAILING RECEIVER (RXDBUF) REGISTER

WHERE YYYYYY IS THE EXPECTED DATA CONTENTS OF THAT REGISTER

WHERE ZZZZZZ IS THE ACTUAL DATA CONTENTS OF THAT REGISTER

6.1.4 PC +2 = TRANSMITTER ERROR PC
REGISTER EXPECTED ACTUAL
1XXXXX YYYYYY ZZZZZZ

WHERE 1XXXXX IS THE ADDRESS OF THE FAILING TRANSMITTER (TXCST) REGISTER

WHERE YYYYYY IS THE EXPECTED CONTENTS OF THAT REGISTER

WHERE ZZZZZZ IS THE ACTUAL CONTENTS OF THAT REGISTER

6.1.5 ERROR DESCRIPTIONS
SEE LISTINGS FOR DETAILS OF ERRORS

6.2 ERROR RECOVERY

6.2.1 SW15 =0
IF THE PROGRAM IS RUN WITH SW15 =0 ,NO OPERATOR ACTION IS
REQUIRED TO CONTINUE TESTING

6.2.2 SW15 =1
IF THE PROGRAM IS RUN WITH SW15 =1 ,TO CONTINUE TESTING
AFTER THE PROGRAM HAS HALTED ,PRESS THE PROCESSOR
CONSOLE "CONTINUE SWITCH"

NOTE: THE PC + 2 OF THE 'HLT' WILL BE DISPLAYED IN THE DATA LIGHTS

6.2.3 ILLEGAL INTERRUPTS
IF AN INTERRUPT OCCURS TO A VECTOR ADDRESS NOT SELECTED
DURING PROGRAM INITIALIZATION, THE PROGRAM WILL HALT IN
THE TRAPCATCHER. THE ADDRESS AT WHICH THE PROGRAM
HALTS IS 2 GREATER THAN THE ADDRESS TO WHICH THE INTERRUPT
OCCURED. THE PROGRAM MUST BE RESTARTED AT 000200 TO
RECOVER FROM THIS ERROR.

6.2.4 ADDITIONAL TROUBLESHOOTING AIDS ERRCNT: & PASCNT:
CHECK THESE TWO TAG LOCATIONS FOR TOTAL # OF ERRORS AND PASSES RESPECTIVELY.
LOADING 000200 AND RESTARTING WILL CLEAR THESE LOCATIONS.

6.3 END OF PASS ROUTINE
THIS TIMEOUT IS MENTIONED HERE FOR CONVENIENCE
IT IS IN THE FORM:

END OF PASS TAPE Y
1XXXXX = DEVICE

WHERE Y IS THE TAPE LOADED

WHERE 1XXXXX IS THE DEVICE'S BASE REGISTER ADDRESS

TO INHIBIT THIS TYPEOUT - TURN TELETYPE OFF

7. RESTRICTIONS

7.1 MULTIPLE DEVICES

UP TO 16(10) DEVICES MAY BE TESTED. HOWEVER, THEY
MUST HAVE CONTIGUOUS ADDRESSES AND VECTORS

NOTE: IF ALL DEVICES UNDER TEST HAVE THE SAME INTERRUPT VECTOR
YOU CAN CHANGE "ZERO: ADD #10,BASEIV ;NEXT BLOCK
(VECTORS)" TO "ZERO: ADD #0,BASEIV";
THEREBY THE VECTOR ADDRESSES WILL NOT BE
UPDATED AFTER EACH PASS.

7.2 DISQUALIFYING DEVICES WHEN RUNNING MULTIPLE DEVICES

WHEN RUNNING MULTIPLE DEVICES AN ACTIVE BIT IS SET
FOR EACH DEVICE RUNNING UNDER TEST IE. BIT 0 FOR
DEVICE 0 ,BIT 15 FOR DEVICE 15
TO DISQUALIFY DEVICES:

7.2.1 IF DEVICE 0 IS TO BE DISQUALIFIED ,SIMPLY RESTART
PROGRAM WITH SW00 =1 AND OMIT THE FIRST DEVICE.

7.2.2 IF HOWEVER, DEVICES 1 THRU 15 OR ANY COMBINATION THEREOF
ARE TO BE DISQUALIFIED....LOAD THE LOCATION OF ACTREG:
OBSERVE THE ACTIVE BITS (ACTIVE =1, NONACTIVE = 0)
AND DEPOSIT 0 WHERE THOSE DEVICES ARE TO BE DISQUALIFIED

7.2.2.1 TO RESTART...TYPE 200G...
THE PROGRAM WILL CONTINUE WITH THE DEVICE IT WAS IN BEFORE HALTING.

7.2.2.2ORSET SW00=1 IN SWITCH REG (LOC. 176) AND TYPE 200G....
ANSWER THE QUESTION :1ST DEVICE : ETC.....
.....THE PROGRAM WILL CONTINUE WITH DEVICE 0

7.2.2.3 IF ALL DEVICES ARE DISQUALIFIED BY MISTAKE THE PROGRAM
WILL TYPEOUT AN ERROR MESSAGE.....TYPE 200G.

7.3 CABLE DELAYS
NOTE: EXTERNAL LOOP BACK TESTS ONLY (MODEM CABLE WITH H315 CONNECTOR ON)

7.3.1 TO PROVIDE SUFFICIENT DELAY FOR CLOCK SIGNAL OVER THE CABLE,
LOCATION "HOLD:" MUST BE MODIFIED TO ACCOMODATE FOR FASTER MACHINES.
PRESENTLY "HOLD:" =20 IS SUFFICIENT TIME ON AN 11/21 MACHINE.

BASICALLY DON'T TRY TO EXCEED 10K TO 12K RATE USING THE EIA DRIVERS

7.4 TO USE THE "XOR" TESTER ,THE BRANCH AROUND THE "XOR"

CODE MUST BE PATCHED TO A 'NOP'. (SEE LISTINGS FOR DETAILS)

- 8. DEFAULT PARAMETERS:
 1ST DEVICE: RECEIVER CONTROL REGISTER ADDRESS- RXCSR: 174300
 VECTOR ADDRESS- DURIV: 330
 ARE YOU RUNNING MULTIPLE DEVICES ?- NO MULTD: 0
 LAST DEVICE: RECEIVER CONTROL REGISTER ADDRESS- LASTADD: 0
 # OF SYNC CHARS SELECTED - 2 SYNCNO: 377
 IS SEC XMIT SWITCH E55-2 ON?- YES SEXMIT: 377
 IS SEC REC SWITCH E55-3 ON?- YES SEREC: 377
 IS OPT CLR ENABLE SWITCH E55-1 ON?- YES OPTCLR: 377
 DO YOU HAVE THE EXTERNAL MODEM BYPASS JUMPER
 CONNECTOR ON (H315)- YES JMRBY: 377

9. PROGRAM DESCRIPTION

- 9.1 THIS PROGRAM PERFORMS THE OFFLINE LOGIC BIT BANGING
 OF THE DEVICE
 SEE LISTING FOR DETAILS

*
 .REM *
 *
 .REM *

10. FLOW CHARTS: RECEIVER FLOW, TRANSMITTER FLOW, TRANSMITTER & RECEIVER FLOW

11. CHANGE HISTORY

NOTE: HISTORY BEGINS WITH REV. C0

REV. C0: 1) ALLOW OPERATOR TO SPECIFY ADDRESS > 170000
 2) INCREASE DELAY VALUE 'HOLD' TO COMPENSATE
 FOR 11/23 EXECUTION TIME (FROM 3777 TO 6200)

CNDUQAO
 IN ORDER TO BE SPECIFIC TO SBC 11/21 PROCESSOR, REV C0
 WAS MODIFIED TO INCLUDE CHANGES FOR PRIORITY 6 INSTEAD OF 7
 AND DEFAULT CSR AND VECTOR ADDRESSES AND ALSO .INIT CALL
 TO CNMAC2.SML INCLUDED AT THE END TO INITIALIZE 11/21
 SPECIFIC VECTORS. THE DIAGNOSTIC WAS RENAMED TO CNDUQAO.
 LISTINGS

12.

*

CNDUQ-AO
CNDUQ4.M11

MACY11 30(1046)
30-OCT-82 12:12

14-DEC-82 09:56 PAGE 58-1
APT COMMUNICATIONS ROUTINE

M 1

SEQ 0012

(1) 000220 105067 000020
(1) 000224 105067 000013
(1) 000230 105067 000006
(3) 000234 012601
(3) 000236 012600
(1) 000240 000207
(1) 000242 000
(1) 000243 000
(1)
(1) 000244 000
(1) 000246
(1) 000200
(1) 000001
(1) 000100
(1) 000040
7262 000001
7388
7392
7427
7444
7457
7469
7482

```
12$:  CLRB  $FFLG      ;;CLEAR FATAL FLAG
      CLRB  $LFLG      ;;CLEAR LOG FLAG
      CLRB  $MFLG      ;;CLEAR MESSAGE FLAG
      MOV   (SP)+,R1    ;;POP STACK INTO R1
      MOV   (SP)+,R0    ;;POP STACK INTO R0
      RTS   PC          ;;RETURN
      $MFLG: .BYTE 0    ;;MESSG. FLAG
      $LFLG: .BYTE 0
      ;;LOG FLAG
      $FFLG: .BYTE 0    ;;FATAL FLAG
      .EVEN
      APTSIZE=200
      APTENV=001
      APTSPool=100
      APTCSUP=040
      $TN=1
```

CNDUQ-AO
CNDUQ4.M11

MACY11 30(1046)
30-OCT-82 12:12

14-DEC-82 09:56 PAGE 61
APT COMMUNICATIONS ROUTINE

N 1

SEQ 0013

7506
7572
7578
7714
7742
7775
7816
7847
7898
7946
7999
8014
8026
8128

8164
8165

.ENABLE ABS

:CNDUQ-AO DUV11 TAPE A
:COPYRIGHT 1977,1980, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754

:STARTING PROCEDURE
:TYPE 200G
:PROGRAM WILL TYPE "CNDUQ-AO DUV11 TAPE A"
:PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
:AT THE END OF A PASS, PROGRAM WILL TYPE "END OF PASS TAPE A"
:AND THEN RESUME TESTING

.SBTTL BASIC DEFINITIONS

;*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***

001100

STACK= 1100
.EQUIV EMT,ERROR ::BASIC DEFINITION OF ERROR CALL
.EQUIV IOT,SCOPE ::BASIC DEFINITION OF SCOPE CALL

;*MISCELLANEOUS DEFINITIONS

000011
000012
000015
000200
177776

HT= 11 ::CODE FOR HORIZONTAL TAB
LF= 12 ::CODE FOR LINE FEED
CR= 15 ::CODE FOR CARRIAGE RETURN
CRLF= 200 ::CODE FOR CARRIAGE RETURN-LINE FEED
PS= 177776 ::PROCESSOR STATUS WORD

177774
177772
177570
177570

.EQUIV PS,PSW
STKLMT= 177774 ::STACK LIMIT REGISTER
PIRQ= 177772 ::PROGRAM INTERRUPT REQUEST REGISTER
DSWR= 177570 ::HARDWARE SWITCH REGISTER
DDISP= 177570 ::HARDWARE DISPLAY REGISTER

170000

***** THE FOLLOWING ODT START ADDRESS FOR SBC 11/21 IS ADDED
ODTST= 170000

;*GENERAL PURPOSE REGISTER DEFINITIONS

000000
000001
000002
000003
000004
000005
000006
000007
000006
000007

R0= %0 ::GENERAL REGISTER
R1= %1 ::GENERAL REGISTER
R2= %2 ::GENERAL REGISTER
R3= %3 ::GENERAL REGISTER
R4= %4 ::GENERAL REGISTER
R5= %5 ::GENERAL REGISTER
R6= %6 ::GENERAL REGISTER
R7= %7 ::GENERAL REGISTER
SP= %6 ::STACK POINTER
PC= %7 ::PROGRAM COUNTER

;*PRIORITY LEVEL DEFINITIONS

000000
000040
000100
000140
000200
000240
000300
000340

PR0= 0 ::PRIORITY LEVEL 0
PR1= 40 ::PRIORITY LEVEL 1
PR2= 100 ::PRIORITY LEVEL 2
PR3= 140 ::PRIORITY LEVEL 3
PR4= 200 ::PRIORITY LEVEL 4
PR5= 240 ::PRIORITY LEVEL 5
PR6= 300 ::PRIORITY LEVEL 6
PR7= 340 ::PRIORITY LEVEL 7

;*SWITCH REGISTER SWITCH DEFINITIONS

100000

SW15= 100000

```

(2)      040000      SW14=  4000
(2)      020000      SW13=  2000
(2)      010000      SW12=  1000
(2)      004000      SW11=   400
(2)      002000      SW10=   200
(2)      001000      SW09=   100
(2)      000400      SW08=    40
(2)      000200      SW07=    20
(2)      000100      SW06=    10
(2)      000040      SW05=     4
(2)      000020      SW04=     2
(2)      000010      SW03=     1
(2)      000004      SW02=     1
(2)      000002      SW01=     1
(2)      000001      SW00=     1
(2)                .EQUIV SW09,SW9
(2)                .EQUIV SW08,SW8
(2)                .EQUIV SW07,SW7
(2)                .EQUIV SW06,SW6
(2)                .EQUIV SW05,SW5
(2)                .EQUIV SW04,SW4
(2)                .EQUIV SW03,SW3
(2)                .EQUIV SW02,SW2
(2)                .EQUIV SW01,SW1
(2)                .EQUIV SW00,SW0
(2)                ;*DATA BIT DEFINITIONS (BIT00 TO BIT15)
(2)      100000      BIT15= 100000
(2)      040000      BIT14=  40000
(2)      020000      BIT13=  20000
(2)      010000      BIT12=  10000
(2)      004000      BIT11=   4000
(2)      002000      BIT10=   2000
(2)      001000      BIT09=   1000
(2)      000400      BIT08=    400
(2)      000200      BIT07=    200
(2)      000100      BIT06=    100
(2)      000040      BIT05=     40
(2)      000020      BIT04=     20
(2)      000010      BIT03=     10
(2)      000004      BIT02=      4
(2)      000002      BIT01=      2
(2)      000001      BIT00=      1
(2)                .EQUIV BIT09,BIT9
(2)                .EQUIV BIT08,BIT8
(2)                .EQUIV BIT07,BIT7
(2)                .EQUIV BIT06,BIT6
(2)                .EQUIV BIT05,BIT5
(2)                .EQUIV BIT04,BIT4
(2)                .EQUIV BIT03,BIT3
(2)                .EQUIV BIT02,BIT2
(2)                .EQUIV BIT01,BIT1
(2)                .EQUIV BIT00,BIT0
(2)                ;*BASIC 'CPU' TRAP VECTOR ADDRESSES
(2)      000004      ERRVEC= 4 ;:TIME OUT AND OTHER ERRORS

```

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(2)      000010      RESVEC= 10      :::RESERVED AND ILLEGAL INSTRUCTIONS
(2)      000014      TBITVEC=14      ::: 'T' BIT
(2)      000014      TRTVEC= 14      :::TRACE TRAP
(2)      000014      BPTVEC= 14      :::BREAKPOINT TRAP (BPT)
(2)      000020      IOTVEC= 20      :::INPUT/OUTPUT TRAP (IOT) **SCOPE**
(2)      000024      PWRVEC= 24      :::POWER FAIL
(2)      000030      EMTVEC= 30      :::EMULATOR TRAP (EMT) **ERROR**
(2)      000034      TRAPVEC=34      ::: 'TRAP' TRAP
(2)      000060      TKVEC= 60      :::TTY KEYBOARD VECTOR
(2)      000064      TPVEC= 64      :::TTY P...INTER VECTOR
(2)      :***** THE FOLLOWING BREAK VECTOR AND LINE CLOCK VECTOR ARE INCLUDED
(2)      000100      LKVEC= 100     :::LINE CLOCK VECTOR
(2)      000140      BRKVEC= 140     :::BREAK VECTOR
(2)      000240      PIRQVEC=240     :::PROGRAM INTERRUPT REQUEST VECTOR

```

```
(2)                               ;STANDARD INTERRUPT VECTORS
(2)
(2)
(2)
(2)   000174   000174           .=174
(2)   000174   000000           DISPREG:0
(2)   000176   000000           SWREG:0
(2)           000200           .=200
(2)   000200   000167   001746   JMP      .START           ;GO TO START OF PROGRAM
(2)
(2)
(2)
(2)           001100           .=1100
(2)   001100   000000           .WORD 0
(2)   001102   177570           LIGHTS:177570
(2)
(2)
(2)                               ;PROGRAM CONTROL PARAMETERS
(2)   001104   000000           RETURN: 0
(2)   001106   000000           NEXT: 0           ;ADDRESS OF NEXT TEST TO BE EXECUTED
(2)   001110   000000           LOCK: 0           ;ADDRESS FOR LOCK ON CURRENT DATA
(2)   001112   000000           PASCNT: 0        ;ADDRESS CONTAINING PASS COUNT
(2)   001114   000000           ERRCNT: 0        ;ERROR COUNT
(2)   001116   000000           SAVSP: 0         ;STACK POINTER STORAGE
(2)
(2)                               ;PROGRAM VARIABLES
(2)   001120   000020           HOLD: 20         ;TEMPORARY STORAGE=DELAY TIME FOR CABLES
(2)   001122   000000           SHIFT: 0        ;TEMPORARY STORAGE= # OF SHIFTS PER CHAR
(2)   001124   000000           COUNT: 0        ;TEMPORARY STORAGE= # OF TIMES A CHAR WILL BE SENT
(2)   001126   000000           SAVPC: 0        ;PROGRAM COUNTER STORAGE
(2)   001130   000000           HLD0: 0
(2)   001132   000000           HLD1: 0
(2)   001134   000000           HLD2: 0
(2)   001136   000000           HLD3: 0
(2)   001140   000000           HLD4: 0
(2)   001142   000000           HLD5: 0
(2)   001144   000000           HLD6: 0
```

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(2)                               ;PROGRAM CONVERSATIONAL PARAMETERS
(2) 001146          377          SYNCNO: .BYTE 377           ;# OF SYNC CHARS REQ'D FOR SYNC'ZATION
(2) 001147          377          SEXMIT: .BYTE 377           ;SEC XMIT JUMPER ''IN''
(2) 001150          377          SEREC:  .BYTE 377           ;SEC REC JUMPER ''IN''
(2) 001151          377          OPTCLR: .BYTE 377           ;OPTIONAL JUMPER CLR ''IN''
(2) 001152          000          MULTD:  .BYTE 0             ;NO MULTIPLE DEVICE FLAG
(2) 001153          377          JMRBY:  .BYTE 377           ;EXTERNAL MODEM BYPASS JUMPER ''IN''
(2)                               .EVEN
(2)
(2)                               ;PROGRAM MULTIPLE DEVICE PARAMETERS
(2) 001154          000000       BASEADD:          0         ;PROG CONTROLLED 1ST DEVICE ADDR
(2) 001156          000000       KEEPADD:         0         ;SAVED 1ST DEVICE ADDR
(2) 001160          000000       LASTADD:         0         ;LAST DEVICE RXCSR ADDR
(2) 001162          000000       BASEIV:          0         ;PROG CONTROLLED IV
(2) 001164          000000       KEEPIV:          0         ;SAVED INTR VECTOR
(2) 001166          000000       ACTREG:          0         ;ACTIVE REGISTER ,,,MODIFY THIS
(2)                               ;LOCATION TO DISQUALIFY OR QUALIFY
(2)                               ;DEVICES (1= RUN,,0= DON'T RUN)
(2) 001170          000000       ROTADD:          0         ;ROTATING POINTER FOR ACTREG..POINTS
(2)                               ;TO DEVICE PRESENTLY UNDER TEST WHEN RUNNING MULTIPLE DEVICES
(2)
(2)                               ;PROGRAM CONTROL FLAGS
(2) 001172          000          INIFLG: .BYTE 0             ;PROGRAM INITIALIZATION FLAG
(2) 001173          000          STFLG:  .BYTE 0             ;TEST START FLAG
(2) 001174          000          LOKFLG: .BYTE 0             ;LOCK ON CURRENT TEST FLAG
(2)                               .EVEN
(1)                               . =1400
(2)
(2)

```


CNDUQ-AO
CNDUQA.M11

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BASIC DEFINITIONS

H 2

SEQ 0020

(2)	000040	DNAINTE=BIT5	:DNA INTR ENAB
(2)	000020	SEND=BIT4	:SEND
(2)	000010	HDXEN=BIT3	:HDX/FDX
(2)	000001	BREAK=BIT0	:BREAK
(2)		:TXCSR WRD DEFINITIONS	
(2)	000000	USER=0	:USER MODE
(2)	004000	MINT=4000	:MAINT INT MODE
(2)	010000	MEXT=10000	:MAINT EXT MODE
(2)	014000	SYSTST=14000	:SYSTEM TEST MODE

(3)	001620	000000	\$DDW3:	.WORD	ADDW3	:::DEVICE	DESCRIPTOR	WORD#3
(3)	001622	000000	\$DDW4:	.WORD	ADDW4	:::DEVICE	DESCRIPTOR	WORD#4
(3)	001624	000000	\$DDW5:	.WORD	ADDW5	:::DEVICE	DESCRIPTOR	WORD#5
(3)	001626	000000	\$DDW6:	.WORD	ADDW6	:::DEVICE	DESCRIPTOR	WORD#6
(3)	001630	000000	\$DDW7:	.WORD	ADDW7	:::DEVICE	DESCRIPTOR	WORD#7
(3)	001632	000000	\$DDW8:	.WORD	ADDW8	:::DEVICE	DESCRIPTOR	WORD#8
(3)	001634	000000	\$DDW9:	.WORD	ADDW9	:::DEVICE	DESCRIPTOR	WORD#9
(3)	001636	000000	\$DDW10:	.WORD	ADDW10	:::DEVICE	DESCRIPTOR	WORD#10
(3)	001640	000000	\$DDW11:	.WORD	ADDW11	:::DEVICE	DESCRIPTOR	WORD#11
(3)	001642	000000	\$DDW12:	.WORD	ADDW12	:::DEVICE	DESCRIPTOR	WORD#12
(3)	001644	000000	\$DDW13:	.WORD	ADDW13	:::DEVICE	DESCRIPTOR	WORD#13
(3)	001646	000000	\$DDW14:	.WORD	ADDW14	:::DEVICE	DESCRIPTOR	WORD#14
(3)	001650	000000	\$DDW15:	.WORD	ADDW15	:::DEVICE	DESCRIPTOR	WORD#15
(3)								
(3)	001652		SETEND:					
(3)								
(4)								
(4)								

```
(4)
(4)
(4)
(4)
(4)          ;INSTRUCTION DEFINITIONS
(4)          005746    PUSH1SP=5746    ;DECREMENT PROCESSOR STACK 1 WORD =TST -(SP)
(4)          005726    POP1SP=5726     ;INCREMENT PROCESSOR STACK 1 WORD =TST (SP)+
(4)          010046    PUSHRO=10046   ;SAVE RO ON STACK =MOV RO,-(SP)
(4)          012600    POPRO=12600    ;RESTORE RO FROM STACK =MOV (SP)+,RO
(4)          024646    PUSH2SP=24646  ;DECREMENT STACK TWICE =CMP -(SP),-(SP)
(4)          022626    POP2SP=22626   ;INCREMENT STACK TWICE =CMP (SP)+,(SP)+
(4)          ;REGISTER DEFINITIONS
(4)          ;RXCSR BIT DEFINITIONS
(4)          100000    DSC=BIT15     ;DATA SET CHANGE
(4)          040000    RING=BIT14    ;RING
(4)          020000    CTS=BIT13     ;CLR TO SEND
(4)          010000    CARDET=BIT12   ;CARRIER DETECT
(4)          004000    REACT=BIT11    ;REC ACTIVE
(4)          002000    SRD=BIT10     ;SEC REC DATA
(4)          001000    DSR=BIT9      ;DATA SET RDY
(4)          000400    STPSYN=BIT8   ;STRIP SYNC
(4)          000200    RXDONE=BIT7   ;REC DONE
(4)          000100    RINTEN=BIT6   ;REC INTR ENABLE
(4)          000040    DSINTE=BIT5   ;DSC INTR ENABLE
(4)          000020    SYN SCH=BIT4   ;SYNC SEARCH
(4)          000010    STD=BIT3      ;SEC XMIT DATA
(4)          000004    RTS=BIT2      ;REQ TO SEND
(4)          000002    DTR=BIT1      ;DATA TERM RDY
(4)          000001    VOID=BIT0
(4)          ;RXDBUF BIT DEFINITIONS
(4)          100000    RXERR=BIT15   ;REC ERROR
(4)          040000    OVRRUN=BIT14  ;OVERRUN
(4)          020000    FRMERR=BIT13   ;FRAME ERROR
(4)          010000    PARER=BIT12   ;PARITY ERROR
(4)          ;PARCSR BIT DEFINITIONS
(4)          001000    PAREN=BIT9    ;PARITY ENABLE
(4)          000400    EVPAR=BIT8    ;EVEN PARITY SENSE
(4)          ;PARCSR WRD DEFINITIONS
(4)          030000    SYNINT=30000  ;SYNC EXTERNAL MODE
(4)          020000    SYNEXT=20000  ;SYNC INTERNAL MODE
(4)          000000    ISYMOD=0      ;ISOC MODE
(4)          000000    FIVE=0        ;WORD LENGTH 5 BITS
(4)          002000    SIX=2000      ;WORD LENGTH 6 BITS
(4)          004000    SEVEN=4000    ;WORD LENGTH 7 BITS
(4)          006000    EIGHT=6000   ;WORD LENGTH 8 BITS
(4)          000000    NOPAR=0       ;NO PARITY
(4)          001000    ODDPAR=1000   ;ODD PARITY
(4)          001400    EVEPAR=1400   ;EVEN PARITY
(4)          ;TXCSR BIT DEFINITIONS
(4)          100000    DNA=BIT15     ;DATA NOT AVAILABLE
(4)          040000    MTDATA=BIT14  ;MAINT DATA
(4)          020000    CLK=BIT13     ;CLK
(4)          002000    BITW=BIT10    ;BIT WINDOW
(4)          000400    MRESET=BIT8   ;MASTER RESET
(4)          000200    TXDONE=BIT7   ;XMIT DONE
(4)          000100    TXINTE=BIT6  ;XMIT INTR ENABLE
```

(4)	000040	DNAINTE=BIT5	:DNA INTR ENAB
(4)	000020	SEND=BIT4	:SEND
(4)	000010	HDXEN=BIT3	:HDX/FDX
(4)	000001	BREAK=BIT0	:BREAK
(4)		;TXCSH WRD DEFINITIONS	
(4)	000000	USER=0	:USER MODE
(4)	004000	MINT=4000	:MAINT INT MODE
(4)	010000	MEXT=10000	:MAINT EXT MODE
(4)	014000	SYSTST=14000	:SYSTEM TEST MODE

```
(2) .SBTTL ERROR POINTER TABLE
(2)
(2) ;*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.
(2) ;*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN
(2) ;*LOCATION $ITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.
(2) ;*NOTE1: IF $ITEMB IS 0 THE ONLY PERTINENT DATA IS ($ERRPC).
(2) ;*NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:
(2)
(2) ;*      EM      ;;POINTS TO THE ERROR MESSAGE
(2) ;*      DH      ;;POINTS TO THE DATA HEADER
(2) ;*      DT      ;;POINTS TO THE DATA
(2) ;*      DF      ;;POINTS TO THE DATA FORMAT
(2)
(2) $ERRTB:
(1) ;ERROR TABLE
(1) 001652 001762 EM1 ;ERROR 1 REGISTER ERROR
(1) 001654 002067 DH1
(1) 001656 002116 DT1
(1) 001660 002132 DF1
(1) 001662 002022 EM2 ;ERROR 2 RECEIVER ERROR
(1) 001664 002067 DH1
(1) 001666 002116 DT1
(1) 001670 002132 DF1
(1) 001672 002043 EM3 ;ERROR 3 TRANSMITTER ERROR
(1) 001674 002067 DH1
(1) 001676 002116 DT1
(1) 001700 002132 DF1
(1) 001702 001746 EM4 ;ERROR 4 BIT ERROR (GENERAL)
(1) 001704 000000 O
(1) 001706 002126 DT4
(1) 001710 002132 DF1
(1)
(1) ;DEFAULT DU ADDRESSES
(1) 001712 174300 RXCSR: 174300
(1) 001714 174301 HRXCSR: 174301
(1) 001716 174302 RXDBUF: 174302
(1) 001720 174303 HRXDBUF: 174303
(1) 001722 174302 PARCSR: 174302
(1) 001724 174303 HPARCSR: 174303
(1) 001726 174304 TXCSR: 174304
(1) 001730 174305 HTXCSR: 174305
(1) 001732 174306 TXDBUF: 174306
(1) 001734 174307 HTXDBUF: 174307
(1)
(1) ;DEFAULT DU VECTORS
(1) 001736 000330 DURIV: 330 ;REC INTR VECTOR
(1) 001740 000332 DURIS: 332 ;REC INTR STATUS
(1) 001742 000334 DUTIV: 334 ;XMIT INTR VECTOR
(1) 001744 000336 DUTIS: 336 ;XMIT INTR STATUS
(1)
(1) ;ERROR MESSAGES
(1) 001746 020040 051105 047522 EM4: .ASCIZ / ERROR PC /
(1) 001754 020122 041520 000040
(1) 001762 020040 047503 050115 EM1: .ASCIZ / COMPARISON ERROR ON REGISTERS/
(1) 001760 051101 051511 047117
(1) 001776 042440 051122 051117
(1) 002004 047440 020116 042522
```



```
(2) 002432 105067 176535          CLRB  STFLG          ;CLEAR START FLAG
(2) 002436 005067 176450          CLR   PASCNT        ;CLEAR PASS COUNT
(2) 002442 105067 176735          CLRB  PERSFLG       ;CLEAR ERROR FLAG
(2) 002446 005067 176740          CLR   $ERRCTL       ;CLEAR ERROR COUNT
(2) 002452 005067 176740          CLR   $ERRPC        ;CLEAR LAST ERROR POINTER
(2) 002456 012767 000001 176716  MOV   #1,$STSTM     ;SET UP FOR TEST 1
(2) 002464 012767 002152 176412  MOV   #.START,RETURN ;SET UP FOR POWER FAIL BEFORE
(2)                                ;TESTING STARTS
(2) 002472 013746 000006          MOV   @#6,-(SP)
(2) 002476 013746 000004          MOV   @#4,-(SP)
(2) 002502 012737 002516 000004  MOV   #1$,@#4
(2) 002510 005777 176724          TST   @SWR
(2) 002514 000407                BR    2$
(2) 002516 012767 000176 176714 1$: MOV   #SWREG,SWR
(2) 002524 012767 000174 176710  MOV   #DISPREG,DISPLAY
(2) 002532 022626                CMP   (SP)+,(SP)+
(2) 002534 012637 000004          MOV   (SP)+,@#4
(2) 002540 012637 000006          MOV   (SP)+,@#6
(2) 002544 022767 000176 176666  CMP   #SWREG,SWR
(2) 002552 001007                BNE   3$
(2) 002554 005737 000042          TST   @#42          ;CHECK FOR CHAIN
(2) 002560 001402                BEQ   33$
(2) 002562 000167 000522          JMP   .BEGIN
(2) 002566 004767 010154 33$: JSR   PC,CNTLU
(2) 002572 105767 176374 3$: TSTB  INIFLG        ;HAS INITIALIZATION BEEN PERFORMED
(2) 002576 001004                BNE   ONCE
(2) 002600 104401 015122          TYPE  ,MTITLE      ;TYPE TITLE MESSAGE
(2) 002604 105167 176362          COMB INIFLG        ;IF NOT SET FLAG AND DO
(2) 002610 105767 176732          ONCE: TSTB $ENV      ;APT CONTROL?
(2) 002614 001410                BEQ   11$          ;BR IF NO
(2) 002616 032767 000001 176726  BIT   #1,$USWR     ;EXTENAL JUMPER ON?
(2) 002624 001002                BNE   12$          ;NO
(2) 002626 105067 176321          CLRB  JMRBY         ;CLEAR FLAG
(2) 002632 000167 000452          JMP   .BEGIN       ;GO DO IT
(2) 002636 032777 000001 176574 11$: BIT   #SW00,@SWR  ;RESELECT VECTOR & CONTROL REG?
(2) 002644 001002                BNE   1$
(2) 002646 000167 000436          JMP   .BEGIN
(2) 002652 012700 000300          1$: MOV   #300,R0 ;RESTORE VECTOR AREA TO TRAPCATCHER
(2) 002656 012701 000302          MOV   #302,R1 ;START AT LOCATION 300
(2) 002662 012702 000004          MOV   #4,R2
(2) 002666 010110          2$: MOV   R1,(R0)
(2) 002670 005011                CLR   (R1)
(2) 002672 060200                ADD   R2,R0
(2) 002674 060201                ADD   R2,R1
(2) 002676 022701 001000          CMP   #1000,R1      ;END AT LOCATION 776
(2) 002702 002771                BLT   2$
(2) 002704 104406          INSTR ;OUTPUT MESSAGE & GET INPUT STRING
(2) 002706 015171          MREGAD ;MESSAGE
(2) 002710 104410          PARAM ;CONVERT STRING
(2) 002712 174000          174000 ;LOW LIMIT
(2) 002714 177776          177776 ;HIGH LIMIT
(2) 002716 017122          DUBASE ;STORE AT THIS LOCATION
(2) 002720 001                .BYTE 1 ;MASK
(2) 002721 001                .BYTE 1 ;HOW MANY TIMES + 2
(1) 002722 016767 014174 176226  MOV   DUBASE,KEEPADD ;SAVE
(1) 002730 004767 014034          JSR   PC,DUADDR
```



```

(1) 003166 012767 000300 013570 OUTMUL: MOV #300,DUPRT
(1) 003174 004767 013514 JSR PC,DULEV
(2) :COMPARE THE FIRST CHARACTER IN THE TELETYPE INPUT
(2) :BUFFER TO THE CHARACTERS '1' AND '2'.
(2) :IF THE CHARACTER IS '1' CLEAR THE FLAG
(2) :IF THE CHARACTER IS '2' SET THE FLAG
(2) 003200 AAA:
(2) 003200 104406 INSTR :OUTPUT MESSAGE & GET INPUT STRING
(2) 003202 015562 MSYNC :MESSAGE
(2) 003204 122767 000061 012712 3$: CMPB #'1,INBUF ;IS IT '1' ?
(2) 003212 001003 BNE 1$
(2) 003214 105067 175726 CLRB SYNCNO ;000
(2) 003220 000412 BR 4$
(2) 003222 122767 000062 012674 1$: CMPB #'2,INBUF ;IS IT '2' ?
(2) 003230 001004 BNE 2$
(2) 003232 112767 177777 175706 MOVB #-1,SYNCNO ;377
(2) 003240 000402 BR 4$
(2) 003242 104407 2$: INSTER :RETRY
(2) 003244 000757 BR 3$
(2) 003246 000240 4$: NOP
(2) 003250 104406 INSTR :OUTPUT MESSAGE & GET INPUT STRING
(2) 003252 015630 MWIRE6 :MESSAGE
(2) 003254 104414 SETFLG :SET FLAG BASED UPON INPUT STRING
(2) 003256 001147 SEXMIT :THIS FLAG
(2) 003260 104406 INSTR :OUTPUT MESSAGE & GET INPUT STRING
(2) 003262 015701 MWIRE5 :MESSAGE
(2) 003264 104414 SETFLG :SET FLAG BASED UPON INPUT STRING
(2) 003266 001150 SEREC :THIS FLAG
(2) 003270 104406 INSTR :OUTPUT MESSAGE & GET INPUT STRING
(2) 003272 015751 MWIRE4 :MESSAGE
(2) 003274 104414 SETFLG :SET FLAG BASED UPON INPUT STRING
(2) 003276 001151 OPTCLR :THIS FLAG
(2) 003300 104406 INSTR :OUTPUT MESSAGE & GET INPUT STRING
(2) 003302 016030 MEXTJ :MESSAGE
(2) 003304 104414 SETFLG :SET FLAG BASED UPON INPUT STRING
(2) 003306 001153 JMRBY :THIS FLAG
(2)
(2) :TEST START AND RESTART
(2)
(2) 003310 012706 001100 .BEGIN: MOV #STACK,SP ;SET UP STACK
(2) 003314 106427 000300 MTPS #300 ;LOCK OUT INTERRUPTS
(2) 003320 032777 000002 176112 BIT #SW01,@SWR ;IF SW01=1, GET STARTING PC
(2) 003326 001413 BEQ 3$
(3) 003330 104406 INSTR :OUTPUT MESSAGE & GET INPUT STRING
(3) 003332 015514 MTSTPC :MESSAGE
(3) 003334 104410 PARAM :CONVERT STRING
(3) 003336 003374 TST1 :LOW LIMIT
(3) 003340 017500 17500 :HIGH LIMIT
(3) 003342 001402 $TSTNM :STORE AT THIS LOCATION
(3) 003344 001 .BYTE 1 :MASK
(3) 003345 001 .BYTE 1 :HOW MANY TIMES + 2
(2) 003346 016767 176030 175530 MOV $TSTNM,RETURN
(2) 003354 000403 BR 4$
(2) 003356 012767 003374 175520 3$: MOV #TST1,RETURN ;START AT TEST 1
(2) 003364 104401 015510 4$: TYPE ,MR ;TYPE R
(2) 003370 000177 175510 JMP @RETURN ;START TESTING

```

```
8166
8167
8168          ;; THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS
(1)          ;;
(5)          ;;*****
(4) 003374 000004      TST1: SCOPE
(4)
(1) 003376 012737 017362 000004      MOV   #TRPREG,@#4      ;SETUP TRAPCATCHER
(1) 003404 016737 174670 000006      MOV   PR6,@#6 ;
(1) 003412 105277 176274                INCB  @RXCSR          ;TEST THIS REG
(1) 003416 000401                BR    .+4             ;IF OK JMP AROUND ERROR
(1) 003420 104004                ERROR 4               ;CHECK DEVICE REG ADDRESSES
(1) 003422 105277 176266                INCB  @HRXCSR ;TEST UPPER BYTE THIS REGISTER
(1) 003426 000401                BR    .+4             ;IF OK JMP AROUND ERROR
(1) 003430 104004                ERROR 4               ;CHECK DEVICE REG ADDRESSES
(1) 003432 012737 000006 000004      MOV   #6,@#4          ;RESTORE TRAPCATCHER
(1) 003440 012737 000000 000006      MOV   #0,@#6          ;
(1)
8169 003446 012767 006200 175444      MOV   #6200,HOLD      ;SET LONGER DELAY FOR TEST.      ;;REV. CO
8170          ;; THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS
(1)          ;;
(5)          ;;*****
(4) 003454 000004      TST2: SCOPE
(4)
(1) 003456 012737 017362 000004      MOV   #TRPREG,@#4      ;SETUP TRAPCATCHER
(1) 003464 016737 174610 000006      MOV   PR6,@#6 ;
(1) 003472 105277 176220                INCB  @RXDBUF         ;TEST THIS REG
(1) 003476 000401                BR    .+4             ;IF OK JMP AROUND ERROR
(1) 003500 104004                ERROR 4               ;CHECK DEVICE REG ADDRESSES
(1) 003502 105277 176212                INCB  @HRXDBUF        ;TEST UPPER BYTE THIS REGISTER
(1) 003506 000401                BR    .+4             ;IF OK JMP AROUND ERROR
(1) 003510 104004                ERROR 4               ;CHECK DEVICE REG ADDRESSES
(1) 003512 012737 000006 000004      MOV   #6,@#4          ;RESTORE TRAPCATCHER
(1) 003520 012737 000000 000006      MOV   #0,@#6          ;
(1)
8171          ;; THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS
(1)          ;;
(5)          ;;*****
(4) 003526 000004      TST3: SCOPE
(4)
(1) 003530 012737 017362 000004      MOV   #TRPREG,@#4      ;SETUP TRAPCATCHER
(1) 003536 016737 174536 000006      MOV   PR6,@#6 ;
(1) 003544 105277 176152                INCB  @PARCSR         ;TEST THIS REG
(1) 003550 000401                BR    .+4             ;IF OK JMP AROUND ERROR
(1) 003552 104004                ERROR 4               ;CHECK DEVICE REG ADDRESSES
(1) 003554 105277 176144                INCB  @HPARCSR        ;TEST UPPER BYTE THIS REGISTER
(1) 003560 000401                BR    .+4             ;IF OK JMP AROUND ERROR
(1) 003562 104004                ERROR 4               ;CHECK DEVICE REG ADDRESSES
(1) 003564 012737 000006 000004      MOV   #6,@#4          ;RESTORE TRAPCATCHER
(1) 003572 012737 000000 000006      MOV   #0,@#6          ;
(1)
8172          ;; THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS
(1)          ;;
(5)          ;;*****
(4) 003600 000004      TST4: SCOPE
(4)
```

```
(1) 003602 012737 017362 000004    MOV    #TRPREG,@#4    ;SETUP TRAPCATCHER
(1) 003610 016737 174464 000006    MOV    PR6,@#6      ;
(1) 003616 105277 176104            INCB   @TXCSR        ;TEST THIS REG
(1) 003622 000401                    BR     .+4           ;IF OK JMP AROUND ERROR
(1) 003624 104004                    ERROR  4             ;CHECK DEVICE REG ADDRESSES
(1) 003626 105277 176076            INCB   @HTXCSR      ;TEST UPPER BYTE THIS REGISTER
(1) 003632 000401                    BR     .+4           ;IF OK JMP AROUND ERROR
(1) 003634 104004                    ERROR  4             ;CHECK DEVICE REG ADDRESSES
(1) 003636 012737 000006 000004    MOV    #6,@#4       ;RESTORE TRAPCATCHER
(1) 003644 012737 000000 000006    MOV    #0,@#6       ;
```

8173 ::THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS

(1) ::
(5) ::*****
(4) 003652 000004 TST5: SCOPE

```
(1) 003654 012737 017362 000004    MOV    #TRPREG,@#4    ;SETUP TRAPCATCHER
(1) 003662 016737 174412 000006    MOV    PR6,@#6      ;
(1) 003670 105277 176036            INCB   @TXDBUF       ;TEST THIS REG
(1) 003674 000401                    BR     .+4           ;IF OK JMP AROUND ERROR
(1) 003676 104004                    ERROR  4             ;CHECK DEVICE REG ADDRESSES
(1) 003700 105277 176030            INCB   @HTXDBUF     ;TEST UPPER BYTE THIS REGISTER
(1) 003704 000401                    BR     .+4           ;IF OK JMP AROUND ERROR
(1) 003706 104004                    ERROR  4             ;CHECK DEVICE REG ADDRESSES
(1) 003710 012737 000006 000004    MOV    #6,@#4       ;RESTORE TRAPCATCHER
(1) 003716 012737 000000 000006    MOV    #0,@#6       ;
```

8174 ::BUS DRIVER TEST

8175 ::
8176 (3) 003724 000004 TST6: SCOPE

```
(3) 003726 022777 000000 175776    CMP    #0,@TXDBUF    ;READING TXDBUF SHOULD BE ALL ZERO'S
8178 003734 001401                    BEQ    .+4           ;
8179 003736 104004                    ERROR  4             ;THIS TEST PERFORMS MASTER RESET TESTING &
8180 ::TESTING OF READ/WRITE BIT DTR
```

(1) ::
(1) ::
(5) ::*****
(4) 003740 000004 TST7: SCOPE

```
(4) (1) 003742 052777 000002 175742    BIS    #DTR,@RXCSR   ;SET THIS BIT
(1) 003750 032777 000002 175734    BIT    #DTR,@RXCSR   ;TEST THIS BIT
(1) 003756 001001                    BNE    .+4           ;BR IF '1'
(1) 003760 104004                    ERROR  4             ;THIS BIT SHOULD BE SET
(1) 003762 042777 000002 175722    BIC    #DTR,@RXCSR   ;CLR THIS BIT
(1) 003770 032777 000002 175714    BIT    #DTR,@RXCSR   ;TEST THIS BIT
(1) 003776 001401                    BEQ    .+4           ;BR IF '0'
(1) 004000 104004                    ERROR  4             ;THIS BIT SHOULD BE CLR
(1) :NOW SET THIS BIT
(1) 004002 052777 000002 175702    BIS    #DTR,@RXCSR   ;
(2) 004010 052777 000400 175710    BIS    #MRESET,@TXCSR ;MASTER RESET
(1) ::CHECK EXISTANCE OF OPTIONAL CLEAR JUMPER
(1) ::
(1) 004016 105767 175127    TSTB  OPTCLR        ;TEST FLAG
(1) 004022 100006    BPL   1$            ;OPTIONAL CLR JUMPER IS NOT IN
```



```

(1) 004216 001001      BNE      .+4      ;BR IF '1'
(1) 004220 104004      ERROR     4          ;THIS BIT SHOULD BE SET
(1) 004222 042777 000010 175462  BIC      #STD,@RXCSR ;CLR THIS BIT
(1) 004230 032777 000010 175454  BIT      #STD,@RXCSR ;TEST THIS BIT
(1) 004236 001401      BEQ      .+4      ;BR IF '0'
(1) 004240 104004      ERROR     4          ;THIS BIT SHOULD BE CLR
(1) ;NOW SET THIS BIT
(1) 004242 052777 000010 175442  BIS      #STD,@RXCSR
(2) 004250 052777 000400 175450  BIS      #MRESET,@TXCSR ;MASTER RESET
(1) ;:CHECK EXISTANCE OF OPTIONAL CLEAR JUMPER
(1) ;:
(1) TSTB      OPTCLR      ;TEST FLAG
(1) 004262 100006      BPL      1$          ;OPTIONAL CLR JUMPER IS NOT IN
(1) 004264 032777 000010 175420  BIT      #STD,@RXCSR ;TEST THIS BIT
(1) 004272 001401      BEQ      .+4      ;BR IF '0'
(1) 004274 104004      ERROR     4          ;CHECK OUT MASTER RESET LOGIC
(1) 004276 000405      BR        2$          ;JMP AROUND
(1) 004300 032777 000010 175404 1$: BIT      #STD,@RXCSR ;TEST THIS BIT
(1) 004306 001001      BNE      .+4      ;BR IF '1'
(1) 004310 104004      ERROR     4          ;CHECK OUT OPTIONAL CLR JUMPER
(1) 004312 000240      2$: NOP
(1)
8184 ;:THIS TEST PERFORMS MASTER RESET TESTING &
(1) ;:TESTING OF READ/WRITE BIT SYNSCH
(1) ;:
(5) ;*****
(4) 004314 000004      TST12: SCOPE
(4)
(1) 004316 052777 000020 175366  BIS      #SYNSCH,@RXCSR ;SET THIS BIT
(1) 004324 032777 000020 175360  BIT      #SYNSCH,@RXCSR ;TEST THIS BIT
(1) 004332 001001      BNE      .+4      ;BR IF '1'
(1) 004334 104004      ERROR     4          ;THIS BIT SHOULD BE SET
(1) 004336 042777 000020 175346  BIC      #SYNSCH,@RXCSR ;CLR THIS BIT
(1) 004344 032777 000020 175340  BIT      #SYNSCH,@RXCSR ;TEST THIS BIT
(1) 004352 001401      BEQ      .+4      ;BR IF '0'
(1) 004354 104004      ERROR     4          ;THIS BIT SHOULD BE CLR
(1) ;NOW SET THIS BIT
(1) 004356 052777 000020 175326  BIS      #SYNSCH,@RXCSR
(2) 004364 052777 000400 175334  BIS      #MRESET,@TXCSR ;MASTER RESET
(1) 004372 032777 000020 175312  BIT      #SYNSCH,@RXCSR ;TEST THIS BIT
(1) 004400 001401      BEQ      .+4      ;BR IF '0'
(1) 004402 104004      ERROR     4          ;CHECK OUT MASTER RESET LOGIC
(1)
8185 ;:THIS TEST PERFORMS MASTER RESET TESTING &
(1) ;:TESTING OF READ/WRITE BIT DSINTE
(1) ;:
(5) ;*****
(4) 004404 000004      TST13: SCOPE
(4)
(1) 004406 052777 000040 175276  BIS      #DSINTE,@RXCSR ;SET THIS BIT
(1) 004414 032777 000040 175270  BIT      #DSINTE,@RXCSR ;TEST THIS BIT
(1) 004422 001001      BNE      .+4      ;BR IF '1'
(1) 004424 104004      ERROR     4          ;THIS BIT SHOULD BE SET
(1) 004426 042777 000040 175256  BIC      #DSINTE,@RXCSR ;CLR THIS BIT
(1) 004434 032777 000040 175250  BIT      #DSINTE,@RXCSR ;TEST THIS BIT
(1) 004442 001401      BEQ      .+4      ;BR IF '0'

```

```

(1) 004444 104004          ERROR 4          ;THIS BIT SHOULD BE CLR
(1)                          ;NOW SET THIS BIT
(1) 004446 052777 000040 175236  BIS    #DSINTE,@RXCSR
(2) 004454 052777 000040 175244  BIS    #MRESET,@TXCSR ;MASTER RESET
(1) 004462 032777 000040 175222  BIT    #DSINTE,@RXCSR ;TEST THIS BIT
(1) 004470 001401          BEQ    .+4          ;BR IF '0'
(1) 004472 104004          ERROR 4          ;CHECK OUT MASTER RESET LOGIC
(1)
8186                          ;: THIS TEST PERFORMS MASTER RESET TESTING &
(1)                          ;: TESTING OF READ/WRITE BIT RINTEN
(1)
(5)                          ;: *****
(4) 004474 000004          TST14: SCOPE
(4)
(1) 004476 052777 000100 175206  BIS    #RINTEN,@RXCSR ;SET THIS BIT
(1) 004504 032777 000100 175200  BIT    #RINTEN,@RXCSR ;TEST THIS BIT
(1) 004512 001001          BNE    .+4          ;BR IF '1'
(1) 004514 104004          ERROR 4          ;THIS BIT SHOULD BE SET
(1) 004516 042777 000100 175166  BIC    #RINTEN,@RXCSR ;CLR THIS BIT
(1) 004524 032777 000100 175160  BIT    #RINTEN,@RXCSR ;TEST THIS BIT
(1) 004532 001401          BEQ    .+4          ;BR IF '0'
(1) 004534 104004          ERROR 4          ;THIS BIT SHOULD BE CLR
(1)                          ;:NOW SET THIS BIT
(1) 004536 052777 000100 175146  BIS    #RINTEN,@RXCSR
(2) 004544 052777 000400 175154  BIS    #MRESET,@TXCSR ;MASTER RESET
(1) 004552 032777 000100 175132  BIT    #RINTEN,@RXCSR ;TEST THIS BIT
(1) 004560 001401          BEQ    .+4          ;BR IF '0'
(1) 004562 104004          ERROR 4          ;CHECK OUT MASTER RESET LOGIC
(1)
8187                          ;: THIS TEST PERFORMS MASTER RESET TESTING &
(1)                          ;: TESTING OF READ/WRITE BIT STPSYN
(1)
(5)                          ;: *****
(4) 004564 000004          TST15: SCOPE
(4)
(1) 004566 052777 000400 175116  BIS    #STPSYN,@RXCSR ;SET THIS BIT
(1) 004574 032777 000400 175110  BIT    #STPSYN,@RXCSR ;TEST THIS BIT
(1) 004602 001001          BNE    .+4          ;BR IF '1'
(1) 004604 104004          ERROR 4          ;THIS BIT SHOULD BE SET
(1) 004606 042777 000400 175076  BIC    #STPSYN,@RXCSR ;CLR THIS BIT
(1) 004614 032777 000400 175070  BIT    #STPSYN,@RXCSR ;TEST THIS BIT
(1) 004622 001401          BEQ    .+4          ;BR IF '0'
(1) 004624 104004          ERROR 4          ;THIS BIT SHOULD BE CLR
(1)                          ;:NOW SET THIS BIT
(1) 004626 052777 000400 175056  BIS    #STPSYN,@RXCSR
(2) 004634 052777 000400 175064  BIS    #MRESET,@TXCSR ;MASTER RESET
(1) 004642 032777 000400 175042  BIT    #STPSYN,@RXCSR ;TEST THIS BIT
(1) 004650 001401          BEQ    .+4          ;BR IF '0'
(1) 004652 104004          ERROR 4          ;CHECK OUT MASTER RESET LOGIC
(1)
8188                          ;: THIS TEST PERFORMS MASTER RESET TESTING &
(1)                          ;: TESTING OF READ/WRITE BIT BREAK
(1)
(5)                          ;: *****
(4) 004654 000004          TST16: SCOPE
(4)

```

```
(1) 004656 052777 000001 175042 BIS #BREAK,@TXCSR ;SET THIS BIT
(1) 004664 032777 000001 175034 BIT #BREAK,@TXCSR ;TEST THIS BIT
(1) 004672 001001 BNE .+4 ;BR IF '1'
(1) 004674 104004 ERROR 4 ;THIS BIT SHOULD BE SET
(1) 004676 042777 000001 175022 BIC #BREAK,@TXCSR ;CLR THIS BIT
(1) 004704 032777 000001 175014 BIT #BREAK,@TXCSR ;TEST THIS BIT
(1) 004712 001401 BEQ .+4 ;BR IF '0'
(1) 004714 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
(1) ;NOW SET THIS BIT
(1) 004716 052777 000001 175002 BIS #BREAK,@TXCSR
(2) 004724 052777 000400 174774 BIS #MRESET,@TXCSR ;MASTER RESET
(1) 004732 032777 000001 174766 BIT #BREAK,@TXCSR ;TEST THIS BIT
(1) 004740 001401 BEQ .+4 ;BR IF '0'
(1) 004742 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
```

8189

:: THIS TEST PERFORMS MASTER RESET TESTING &
:: TESTING OF READ/WRITE BIT HDXEN

TST17: SCOPE

```
(1) ;
(1) ;
(5) ;
(4) 004744 000004
(4) ;
(1) 004746 052777 000010 174752 BIS #HDXEN,@TXCSR ;SET THIS BIT
(1) 004754 032777 000010 174744 BIT #HDXEN,@TXCSR ;TEST THIS BIT
(1) 004762 001001 BNE .+4 ;BR IF '1'
(1) 004764 104004 ERROR 4 ;THIS BIT SHOULD BE SET
(1) 004766 042777 000010 174732 BIC #HDXEN,@TXCSR ;CLR THIS BIT
(1) 004774 032777 000010 174724 BIT #HDXEN,@TXCSR ;TEST THIS BIT
(1) 005002 001401 BEQ .+4 ;BR IF '0'
(1) 005004 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
(1) ;NOW SET THIS BIT
(1) 005006 052777 000010 174712 BIS #HDXEN,@TXCSR
(2) 005014 052777 000400 174704 BIS #MRESET,@TXCSR ;MASTER RESET
(1) 005022 032777 000010 174676 BIT #HDXEN,@TXCSR ;TEST THIS BIT
(1) 005030 001401 BEQ .+4 ;BR IF '0'
(1) 005032 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
```

8190

:: THIS TEST PERFORMS MASTER RESET TESTING &
:: TESTING OF READ/WRITE BIT SEND

TST20: SCOPE

```
(1) ;
(1) ;
(5) ;
(4) 005034 000004
(4) ;
(1) 005036 052777 000020 174662 BIS #SEND,@TXCSR ;SET THIS BIT
(1) 005044 032777 000020 174654 BIT #SEND,@TXCSR ;TEST THIS BIT
(1) 005052 001001 BNE .+4 ;BR IF '1'
(1) 005054 104004 ERROR 4 ;THIS BIT SHOULD BE SET
(1) 005056 042777 000020 174642 BIC #SEND,@TXCSR ;CLR THIS BIT
(1) 005064 032777 000020 174634 BIT #SEND,@TXCSR ;TEST THIS BIT
(1) 005072 001401 BEQ .+4 ;BR IF '0'
(1) 005074 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
(1) ;NOW SET THIS BIT
(1) 005076 052777 000020 174622 BIS #SEND,@TXCSR
(2) 005104 052777 000400 174614 BIS #MRESET,@TXCSR ;MASTER RESET
(1) 005112 032777 000020 174606 BIT #SEND,@TXCSR ;TEST THIS BIT
(1) 005120 001401 BEQ .+4 ;BR IF '0'
(1) 005122 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
```

```

(1)
8191          ::THIS TEST PERFORMS MASTER RESET TESTING &
(1)          ::TESTING OF READ/WRITE BIT DINAITE
(1)          ::
(5)          ::*****
(4) 005124   000004   TST21: SCOPE
(4)
(1) 005126   052777   000040   174572   BIS   #DNAITE,@TXCSR ;SET THIS BIT
(1) 005134   032777   000040   174564   BIT   #DNAITE,@TXCSR ;TEST THIS BIT
(1) 005142   001001                   BNE   .+4 ;BR IF '1'
(1) 005144   104004                   ERROR  4 ;THIS BIT SHOULD BE SET
(1) 005146   042777   000040   174552   BIC   #DNAITE,@TXCSR ;CLR THIS BIT
(1) 005154   032777   000040   174544   BIT   #DNAITE,@TXCSR ;TEST THIS BIT
(1) 005162   001401                   BEQ   .+4 ;BR IF '0'
(1) 005164   104004                   ERROR  4 ;THIS BIT SHOULD BE CLR
(1)          :NOW SET THIS BIT
(1) 005166   052777   000040   174532   BIS   #DNAITE,@TXCSR
(2) 005174   052777   000400   174524   BIS   #MRESET,@TXCSR ;MASTER RESET
(1) 005202   032777   000040   174516   BIT   #DNAITE,@TXCSR ;TEST THIS BIT
(1) 005210   001401                   BEQ   .+4 ;BR IF '0'
(1) 005212   104004                   ERROR  4 ;CHECK OUT MASTER RESET LOGIC
(1)
8192          ::THIS TEST PERFORMS MASTER RESET TESTING &
(1)          ::TESTING OF READ/WRITE BIT TXINTE
(1)          ::
(5)          ::*****
(4) 005214   000004   TST22: SCOPE
(4)
(1) 005216   052777   000100   174502   BIS   #TXINTE,@TXCSR ;SET THIS BIT
(1) 005224   032777   000100   174474   BIT   #TXINTE,@TXCSR ;TEST THIS BIT
(1) 005232   001001                   BNE   .+4 ;BR IF '1'
(1) 005234   104004                   ERROR  4 ;THIS BIT SHOULD BE SET
(1) 005236   042777   000100   174462   BIC   #TXINTE,@TXCSR ;CLR THIS BIT
(1) 005244   032777   000100   174454   BIT   #TXINTE,@TXCSR ;TEST THIS BIT
(1) 005252   001401                   BEQ   .+4 ;BR IF '0'
(1) 005254   104004                   ERROR  4 ;THIS BIT SHOULD BE CLR
(1)          :NOW SET THIS BIT
(1) 005256   052777   000100   174442   BIS   #TXINTE,@TXCSR
(2) 005264   052777   000400   174434   BIS   #MRESET,@TXCSR ;MASTER RESET
(1) 005272   032777   000100   174426   BIT   #TXINTE,@TXCSR ;TEST THIS BIT
(1) 005300   001401                   BEQ   .+4 ;BR IF '0'
(1) 005302   104004                   ERROR  4 ;CHECK OUT MASTER RESET LOGIC
(1)
8193          ::TEST MAINT MODE BIT 0
8194          ::
8195          ::THIS TEST PERFORMS MASTER RESET TESTING &
(1)          ::TESTING OF READ/WRITE BIT BIT11
(1)          ::
(5)          ::*****
(4) 005304   000004   TST23: SCOPE
(4)
(1) 005306   052777   004000   174412   BIS   #BIT11,@TXCSR ;SET THIS BIT
(1) 005314   032777   004000   174404   BIT   #BIT11,@TXCSR ;TEST THIS BIT
(1) 005322   001001                   BNE   .+4 ;BR IF '1'
(1) 005324   104004                   ERROR  4 ;THIS BIT SHOULD BE SET
(1) 005326   042777   004000   174372   BIC   #BIT11,@TXCSR ;CLR THIS BIT

```

```

(1) 005334 032777 004000 174364 BIT #BIT11,@TXCSR ;TEST THIS BIT
(1) 005342 001401 BEQ .+4 ;BR IF '0'
(1) 005344 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
(1) ;NOW SET THIS BIT
(1) 005346 052777 004000 174352 BIS #BIT11,@TXCSR
(2) 005354 052777 000400 174344 BIS #MRESET,@TXCSR ;MASTER RESET
(1) 005362 032777 004000 174336 BIT #BIT11,@TXCSR ;TEST THIS BIT
(1) 005370 001401 BEQ .+4 ;BR IF '0'
(1) 005372 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
(1)
8196 ;:TEST MAINT MODE BIT 1
8197 ;:
8198 ;:THIS TEST PERFORMS MASTER RESET TESTING &
(1) ;:TESTING OF READ/WRITE BIT BIT12
(1) ;:
(5) ;:*****
(4) 005374 000004 TST24: SCOPE
(4)
(1) 005376 052777 010000 174322 BIS #BIT12,@TXCSR ;SET THIS BIT
(1) 005404 032777 010000 174314 BIT #BIT12,@TXCSR ;TEST THIS BIT
(1) 005412 001001 BNE .+4 ;BR IF '1'
(1) 005414 104004 ERROR 4 ;THIS BIT SHOULD BE SET
(1) 005416 042777 010000 174302 BIC #BIT12,@TXCSR ;CLR THIS BIT
(1) 005424 032777 010000 174274 BIT #BIT12,@TXCSR ;TEST THIS BIT
(1) 005432 001401 BEQ .+4 ;BR IF '0'
(1) 005434 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
(1) ;NOW SET THIS BIT
(1) 005436 052777 010000 174262 BIS #BIT12,@TXCSR
(2) 005444 052777 000400 174254 BIS #MRESET,@TXCSR ;MASTER RESET
(1) 005452 032777 010000 174246 BIT #BIT12,@TXCSR ;TEST THIS BIT
(1) 005460 001401 BEQ .+4 ;BR IF '0'
(1) 005462 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
(1)
8199 ;:THIS TEST PERFORMS MASTER RESET TESTING &
(1) ;:TESTING OF READ/WRITE BIT CLK
(1) ;:
(5) ;:*****
(4) 005464 000004 TST25: SCOPE
(4)
(1) 005466 052777 020000 174232 BIS #CLK,@TXCSR ;SET THIS BIT
(1) 005474 032777 020000 174224 BIT #CLK,@TXCSR ;TEST THIS BIT
(1) 005502 001001 BNE .+4 ;BR IF '1'
(1) 005504 104004 ERROR 4 ;THIS BIT SHOULD BE SET
(1) 005506 042777 020000 174212 BIC #CLK,@TXCSR ;CLR THIS BIT
(1) 005514 032777 020000 174204 BIT #CLK,@TXCSR ;TEST THIS BIT
(1) 005522 001401 BEQ .+4 ;BR IF '0'
(1) 005524 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
(1) ;NOW SET THIS BIT
(1) 005526 052777 020000 174172 BIS #CLK,@TXCSR
(2) 005534 052777 000400 174164 BIS #MRESET,@TXCSR ;MASTER RESET
(1) 005542 032777 020000 174156 BIT #CLK,@TXCSR ;TEST THIS BIT
(1) 005550 001401 BEQ .+4 ;BR IF '0'
(1) 005552 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
(1)
8200 ;:THIS TEST PERFORMS MASTER RESET TESTING &
(1) ;:TESTING OF READ/WRITE BIT MTDATA

```

```
(1)
(5)
(4) 005554 000004
(4)
(1) 005556 052777 040000 174142
(1) 005564 032777 040000 174134
(1) 005572 001001
(1) 005574 104004
(1) 005576 042777 040000 174122
(1) 005604 032777 040000 174114
(1) 005612 001401
(1) 005614 104004
(1)
(1) 005616 052777 040000 174102
(2) 005624 052777 000400 174074
(1) 005632 032777 040000 174066
(1) 005640 001401
(1) 005642 104004
(1)
8201
8202
8203
8204
(3) 005644 000004
(3)
8205 005646 012777 177777 174036
8206 005654 012777 177777 174044
8207 005662 000005
8208 005664 106427 000300
8209 005670 017701 174016
8210 005674 017702 174026
8211 005700 105767 173245
8212 005704 100402
8213 005706 042701 000016
8214 005712 042701 073000
8215 005716 005701
8216 005720 001401
8217 005722 104004
8218 005724 042702 002200
8219 005730 005702
8220 005732 001401
8221 005734 104004
8222
(1)
(1)
(1)
(1) 005736 016702 173156
(1) 005742 005302
(1) 005744 001376
(1)
(1)
8223
8224
(1)
(1)
(5)
```

```

:*****:
TST26: SCOPE
BIS #MTDATA,@TXCSR ;SET THIS BIT
BIT #MTDATA,@TXCSR ;TEST THIS BIT
BNE .+4 ;BR IF '1'
ERROR 4 ;THIS BIT SHOULD BE SET
BIC #MTDATA,@TXCSR ;CLR THIS BIT
BIT #MTDATA,@TXCSR ;TEST THIS BIT
BEQ .+4 ;BR IF '0'
ERROR 4 ;THIS BIT SHOULD BE CLR
:NOW SET THIS BIT
BIS #MTDATA,@TXCSR
BIS #MRESET,@TXCSR ;MASTER RESET
BIT #MTDATA,@TXCSR ;TEST THIS BIT
BEQ .+4 ;BR IF '0'
ERROR 4 ;CHECK OUT MASTER RESET LOGIC

:THIS TEST VERIFYS THAT INIT (RESET) CLEARS BITS IN THE
:RXCSR & TXCSR
:*****:
TST27: SCOPE
MOV #177777,@RXCSR ;SET ALL POSSIBLE BITS
MOV #177777,@TXCSR ;DITTO
RESET
MTPS #300 ;RESTORE NON INTERRUPT STATUS
MOV @RXCSR,R1 ;SAVE
MOV @TXCSR,R2 ;SAVE
TSTB OPTCLR ;IS THE OPTIONAL CLR JUMPER ON ?
BMI 1$ ;YES
BIC #16,R1 ;CLR THE NON RESETABLE BITS
1$: BIC #073000,R1 ;CLR ALL NON-CLEARABLE BITS
TST R1 ;ARE THEY ALL 0 ?
BEQ .+4
ERROR 4 ;ALL SPECIFIED BITS SHOULD BE CLEAR
BIC #002200,R2 ;CLEAR ALL NON-CLEARABLE BITS
TST R2 ;ARE THEY ALL 0 ?
BEQ .+4
ERROR 4 ;ALL SPECIFIED BITS SHOULD BE CLEAR
:WAIT FOR CABLE DELAYS
:*****:
:MODIFY 'HOLD:' ACCORDINGLY FOR FASTER OR SLOWER MACHINE
:*****:
MOV HOLD,R2 ;SET DELAY TIME
DEC R2
BNE .-2 ;WAIT THIS TIME
:OK NOW FALL THRU AND CONTINUE TESTING.....
:EXIT STAGE LEFT....CHINNG!

:THIS TEST PERFORMS MASTER RESET TESTING &
:TESTING OF WRITE ONLY BIT MRESET
:*****:
```

```
(4) 005746 000004           TST30: SCOPE  
(4)  
(1) 005750 052777 000400 173750        BIS   #MRESET,@TXCSR  ;TRY TO SET THIS BIT  
(1) 005756 032777 000400 173742        BIT   #MRESET,@TXCSR  ;TEST THIS BIT  
(1) 005764 001401                  BEQ   .+4               ;BR IF '0'  
(1) 005766 104004                  ERROR  4                 ;THIS BIT SHOULD NOT BE SET  
(2) 005770 052777 000400 173730        BIS   #MRESET,@TXCSR  ;MASTER RESET  
(1) 005776 032777 000400 173722        BIT   #MRESET,@TXCSR  ;TEST THIS BIT  
(1) 006004 001401                  BEQ   .+4               ;BR IF '0'  
(1) 006006 104004                  ERROR  4                 ;THIS BIT SHOULD NOT BE SET  
(1)                                   ;CHECK MASTER RESET LOGIC  
(1)  
8225                               ;:THIS TEST VERIFYS THAT THE RXCSR & TXCSR CAN BE BYTE ADDRESSED (DATOB)  
8226                               ;:  
8227                               ;:*****  
(3) 006010 000004           TST31: SCOPE  
(3)  
8228 006012 052777 000400 173706        BIS   #MRESET,@TXCSR  ;MASTER RESET  
8229 006020 105767 173125                TSTB  OPTCLR           ;IS THE OPTIONAL CLR JUMPER ON ?  
8230 006024 100405                BMI   1$               ;YES  
8231 006026 012777 000000 173656        MOV   #0,@RXCSR        ;CLR OUT NON RESETABLE BITS  
8232 006034 005777 173652                TST  @RXCSR           ;CLR OUT DSC BY READING RXCSR  
8233 006040 152777 000001 173646 1$:   BISB  #BIT0,@HRXCSR    ;SET STRIP SYNC UPPER BYTE  
8234 006046 017701 173640                MOV   @RXCSR,R1        ;SAVE RXCSR  
8235 006052 022701 000400                CMP   #40C,R1          ;TEST RXCSR  
8236 006056 001401                  BEQ   .+4  
8237 006060 104004                  ERROR  4                 ;ONLY STRIP SYNC SHOULD BE SET  
8238 006062 105077 173624                CLRB  @RXCSR           ;CLR LOWER BYTE  
8239 006066 017701 173620                MOV   @RXCSR,R1        ;SAVE RXCSR  
8240 006072 022701 000400                CMP   #400,R1          ;TEST RXCSR  
8241 006076 001401                  BEQ   .+4  
8242 006100 104004                  ERROR  4                 ;ONLY STRIP SYNC SHOULD BE SET  
8243 006102 052777 000400 173616        BIS   #MRESET,@TXCSR  ;MASTER RESET  
8244 006110 152777 000040 173612        BISB  #BIT5,@HTXCSR   ;SET MAINT CLK UPPER BYTE  
8245 006116 017701 173604                MOV   @TXCSR,R1        ;SAVE TXCSR  
8246 006122 042701 002000                BIC   #BITW,R1         ;CLR BIT WINDOW (DEPENDENT  
8247                                   ;ON H315 CONNECTOR EXISTANCE)  
8248 006126 022701 020200                CMP   #20200,R1        ;TEST TXCSR  
8249 006132 001401                  BEQ   .+4  
8250 006134 104004                  ERROR  4                 ;ONLY MAINT CLK BIT & TXDONE SHOULD BE SET  
8251 006136 105077 173564                CLRB  @TXCSR           ;CLR LOWER BYTE  
8252 006142 017701 173560                MOV   @TXCSR,R1        ;SAVE TXCSR  
8253 006146 042701 002000                BIC   #BITW,R1         ;CLR BIT WINDOW (DITTO)  
8254 006152 022701 020200                CMP   #20200,R1        ;TEST TXCSR  
8255 006156 001401                  BEQ   .+4  
8256 006160 104004                  ERROR  4                 ;ONLY MAINT CLK BIT & TXDONE SHOULD BE SET  
8257                               ;:THIS TEST PERFORMS MASTER RESET TESTING &  
8258                               ;:TESTING OF READ ONLY BIT BITW  
8259                               ;:MAINT INTERNAL  
8260                               ;:  
8261                               ;:*****  
(3) 006162 000004           TST32: SCOPE  
(3)  
8262 006164 012777 044001 173534        MOV   #MINT!MTDATA!BREAK,@TXCSR ;SET MAINT INT.,BREAK,  
8263                                   ;&MTDATA  
8264 006172 032777 002000 173526        BIT   #BITW,@TXCSR    ;TEST BITW
```



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(1) 006414 032777 000200 173270      BIT    #RXDONE,@RXCSR  ;TEST THIS BIT
(1) 006422 001401                      BEQ    .+4              ;BR IF '0'
(1) 006424 104004                      ERROR  4                ;CHECK MASTER RESET LOGIC
(1)                                     ;OR SHORT ON THIS BIT
(1)
8313                                     ::THIS TEST PERFORMS MASTER RESET TESTING &
(1)                                     ::TESTING OF READ ONLY BIT REACT
(1)
(5)                                     ::*****
(4) 006426 000004      TST35:  SCOPE
(4)
(2) 006430 052777 000400 173270      BIS    #MRESET,@TXCSR ;MASTER RESET
(1) 006436 032777 004000 173246      BIT    #REACT,@RXCSR  ;TEST THIS BIT
(1) 006444 001401                      BEQ    .+4              ;BR IF '0'
(1) 006446 104004                      ERROR  4                ;CHECK MASTER RESET LOGIC
(1)                                     ;OR SHORT ON THIS BIT
(1)
8314                                     ::THIS TEST PERFORMS MASTER RESET TESTING &
(1)                                     ::TESTING OF READ ONLY BIT DSC
(1)
(5)                                     ::*****
(4) 006450 000004      TST36:  SCOPE
(4)
(2) 006452 052777 000400 173246      BIS    #MRESET,@TXCSR ;MASTER RESET
(1) 006460 032777 100000 173224      BIT    #DSC,@RXCSR    ;TEST THIS BIT
(1) 006466 001401                      BEQ    .+4              ;BR IF '0'
(1) 006470 104004                      ERROR  4                ;CHECK MASTER RESET LOGIC
(1)                                     ;OR SHORT ON THIS BIT
(1)
8315                                     ::THIS TEST PERFORMS MASTER RESET TESTING &
8316                                     ::TESTING OF READ ONLY BIT TXDONE
8317
8318                                     ::*****
(3) 006472 000004      TST37:  SCOPE
(3)
8319 006474 052777 000400 173224      BIS    #MRESET,@TXCSR ;MASTER RESET
8320 006502 032777 000200 173216      BIT    #TXDONE,@TXCSR ;TEST THIS BIT
8321 006510 001001                      BNE    .+4              ;BR IF '1'
8322 006512 104004                      ERROR  4                ;CHECK MASTER RESET LOGIC
8323                                     ;OR SHORT ON THIS BIT
8324                                     ::THIS TEST PERFORMS MASTER RESET TESTING &
(1)                                     ::TESTING OF READ ONLY BIT DNA
(1)
(5)                                     ::*****
(4) 006514 000004      TST40:  SCOPE
(4)
(2) 006516 052777 000400 173202      BIS    #MRESET,@TXCSR ;MASTER RESET
(1) 006524 032777 100000 173174      BIT    #DNA,@TXCSR    ;TEST THIS BIT
(1) 006532 001401                      BEQ    .+4              ;BR IF '0'
(1) 006534 104004                      ERROR  4                ;CHECK MASTER RESET LOGIC
(1)                                     ;OR SHORT ON THIS BIT
(1)
8325                                     ::THIS TEST PERFORMS MASTER RESET TESTING &
8326                                     ::TESTING OF READ ONLY WORD RECEIVE DATA
8327
8328                                     ::*****

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(3) 006536 000004 TST41: SCOPE  
(3)  
8329 006540 052777 000400 173160 BIS #MRESET,@TXCSR ;MASTER RESET  
8330 006546 016703 173144 MOV RXDBUF,R3 ;FOR ERROR MESSAGE  
8331 006552 012700 000377 MOV #377,R0 ;EXPECTED  
8332 006556 017701 173134 MOV @RXDBUF,R1 ;ACTUAL  
8333 006562 120001 CMPB R0,R1  
8334 006564 001401 BEQ .+4 ;BR IF '0'  
8335 006566 104002 ERROR 2 ;REC DATA SHOULD BE ALL 1'S  
8336  
: THIS TEST PERFORMS MASTER RESET TESTING &  
: TESTING OF READ ONLY BIT PARER  
: : :  
: *****  
(4) 006570 000004 TST42: SCOPE  
(4)  
(2) 006572 052777 000400 173126 BIS #MRESET,@TXCSR ;MASTER RESET  
(1) 006600 032777 010000 173110 BIT #PARER,@RXDBUF ;TEST THIS BIT  
(1) 006606 001401 BEQ .+4 ;BR IF '0'  
(1) 006610 104004 ERROR 4 ;CHECK MASTER RESET LOGIC  
(1) ;OR SHORT ON THIS BIT  
(1)  
8337 : THIS TEST PERFORMS MASTER RESET TESTING &  
(1) : TESTING OF READ ONLY BIT FRMERR  
(1) : :  
(5) : *****  
(4) 006612 000004 TST43: SCOPE  
(4)  
(2) 006614 052777 000400 173104 BIS #MRESET,@TXCSR ;MASTER RESET  
(1) 006622 032777 020000 173066 BIT #FRMERR,@RXDBUF ;TEST THIS BIT  
(1) 006630 001401 BEQ .+4 ;BR IF '0'  
(1) 006632 104004 ERROR 4 ;CHECK MASTER RESET LOGIC  
(1) ;OR SHORT ON THIS BIT  
(1)  
8338 : THIS TEST PERFORMS MASTER RESET TESTING &  
(1) : TESTING OF READ ONLY BIT OVRRUN  
(1) : :  
(5) : *****  
(4) 006634 000004 TST44: SCOPE  
(4)  
(2) 006636 052777 000400 173062 BIS #MRESET,@TXCSR ;MASTER RESET  
(1) 006644 032777 040000 173044 BIT #OVRRUN,@RXDBUF ;TEST THIS BIT  
(1) 006652 001401 BEQ .+4 ;BR IF '0'  
(1) 006654 104004 ERROR 4 ;CHECK MASTER RESET LOGIC  
(1) ;OR SHORT ON THIS BIT  
(1)  
8339 : THIS TEST PERFORMS MASTER RESET TESTING &  
(1) : TESTING OF READ ONLY BIT RXERR  
(1) : :  
(5) : *****  
(4) 006656 000004 TST45: SCOPE  
(4)  
(2) 006660 052777 000400 173040 BIS #MRESET,@TXCSR ;MASTER RESET  
(1) 006666 032777 100000 173022 BIT #RXERR,@RXDBUF ;TEST THIS BIT  
(1) 006674 001401 BEQ .+4 ;BR IF '0'  
(1) 006676 104004 ERROR 4 ;CHECK MASTER RESET LOGIC  
(1) ;OR SHORT ON THIS BIT
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8383
8384                ;:
(3) 007042 000004  ;*****
(3)                TST50: SCOPE
8385 007044 052777 000400 172654     BIS      #MRESET,@TXCSR ;MASTER RESET
8386 007052 016703 172640            MOV      RXDBUF,R3      ;FOR ERROR MESSAGE
8387 007056 017701 172634            MOV      @RXDBUF,R1    ;SAVE
8388 007062 012700 000377            MOV      #377,R0      ;EXPECTED
8389 007066 020001                        CMP      R0,R1        ;EXPECTED VS ACTUAL
8390 007070 001401                        BEQ      .+4
8391 007072 104002                        ERROR 2          ;ONLY REC DATA BITS SHOULD BE SET
8392                    ;:THIS TEST VERIFYS BITS RING,CTS,CARDET,SRD,DSR
8393                    ;:ALSO DSC IS GENERATED WHEN ANY OF THESE BITS ARE SET
8394                    ;:OR CLEARED.....IT ALSO CHECKS THE MODEM BYPASS
8395                    ;:JUMPER AND THAT THESE BITS CAN BE READ
8396                    ;:NOTE: THE MODEM BYPASS JUMPER MUST BE ON (H315)
8397                    ;:
8398                ;*****
(3) 007074 000004  ;TST51: SCOPE
(3)
8399 007076 005077 172610            CLR      @RXCSR ;TO GET RID OF STD ,RTS,DTR IF OPTCLR JUMPER #4 IS NOT ON
8400 007102 052777 000400 172616     BIS      #MRESET,@TXCSR ;MASTER RESET
8401                    ;:TEST THAT A 'YES' ANSWER WAS GIVEN TO QUESTION IN
8402                    ;:THE MONITOR OR BY DEFAULT
8403                    ;:THIS TEST WILL BE BYPASSED IF THE EXTERNAL BYPASS
8404                    ;:JUMPER IS NOT INSTALLED
8405 007110 105767 172037            TSTB    JMRBY
8406 007114 100402                        BMI      .+6          ;THE ANSWER WAS YES.....
8407                    ;:PERFORM THIS TEST
8408 007116 000167 000652            JMP      OUT1         ;JUMP AROUND THIS TEST IF THE ANSWER
8409                    ;:WAS NO
8410 007122 016703 172564            MOV      RXCSR,R3     ;SET UP FOR ERROR MESSAGE
8411 007126 017701 172560            MOV      @RXCSR,R1    ;ACTUAL
8412 007132 005000                        CLR      R0           ;EXPECTED
8413 007134 005701                        TST      R1           ;IS IT = 0 ?
8414 007136 001401                        BEQ      .+4
8415 007140 104001                        ERROR 1          ;RXCSR SHOULD BE CLR
8416 007142 052777 000002 172542     BIS      #DTR,@RXCSR  ;SET DTR
8417                    ;:WAIT FOR CABLE DELAYS
(1)                    ;*****
(1)                    ;:MODIFY 'HOLD:' ACCORDINGLY FOR FASTER OR SLOWER MACHINE
(1)                    ;*****
(1) 007150 016702 171744            MOV      HOLD,R2     ;SET DELAY TIME
(1) 007154 005302                        DEC      R2
(1) 007156 001376                        BNE     .-2          ;WAIT THIS TIME
(1)                    ;:OK NOW FALL THRU AND CONTINUE TESTING.....
(1)                    ;:EXIT STAGE LEFT....CHINNG!
8418 007160 017701 172526            MOV      @RXCSR,R1    ;ACTUAL
8419 007164 012700 130002            MOV      #130002,R0   ;DSC,CTS,CARDET,DTR
8420 007170 020001                        CMP      R0,R1        ;EXPECTED VS ACTUAL
8421 007172 001401                        BEQ      .+4
8422 007174 104001                        ERROR 1          ;CHECK BYPASS CONNECTOR
8423 007176 017701 172510            MOV      @RXCSR,R1    ;ACTUAL
8424 007202 012700 030002            MOV      #30002,R0    ;CTS,CARDET,DTR
8425 007206 020001                        CMP      R0,R1        ;EXPECTED VS ACTUAL
8426 007210 001401                        BEQ      .+4

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(1) ;OK NOW FALL THRU AND CONTINUE TESTING.....
(1) ;EXIT STAGE LEFT....CHINNG!
8493 007536 017701 172150 MOV @RXCSR,R1 ;ACTUAL
8494 007542 012700 070016 MOV #70016,R0 ;EXPECTED: RING ,CTS,CARDET,STD,RTS,DTR
8495 007546 020001 CMP R0,R1 ;EXPECTED VS ACTUAL
8496 007550 001401 BEQ +4
8497 007552 104001 ERROR 1 ;CHECK SEC XMIT & SEC REC JUMPERS
8498 007554 042777 000004 172130 BIC #RTS,@RXCSR
8499 ;WAIT FOR CABLE DELAYS
(1) ;*****
(1) ;MODIFY 'HOLD:' ACCORDINGLY FOR FASTER OR SLOWER MACHINE
(1) ;*****
(1) 007562 016702 171332 MOV HOLD,R2 ;SET DELAY TIME
(1) 007566 005302 DEC R2
(1) 007570 001376 BNE -2 ;WAIT THIS TIME
(1) ;OK NOW FALL THRU AND CONTINUE TESTING.....
(1) ;EXIT STAGE LEFT....CHINNG!
8500 007572 017701 172114 MOV @RXCSR,R1 ;ACTUAL
8501 007576 012700 130012 MOV #130012,R0 ;DSC,CTS,CARDET,DTR,STD
8502 ;NOTE THAT DSC STILL ASSERTS EVEN THO THE SEC XMIT JUMPER # 6 IS NOT ON
8503 007602 020001 CMP R0,R1 ;EXPECTED VS ACTUAL
8504 007604 001401 BEQ +4
8505 007606 104001 ERROR 1 ;CHECK BYPASS CONNECTOR
8506 007610 042777 000002 172074 BIC #DTR,@RXCSR
8507 ;WAIT FOR CABLE DELAYS
(1) ;*****
(1) ;MODIFY 'HOLD:' ACCORDINGLY FOR FASTER OR SLOWER MACHINE
(1) ;*****
(1) 007616 016702 171276 MOV HOLD,R2 ;SET DELAY TIME
(1) 007622 005302 DEC R2
(1) 007624 001376 BNE -2 ;WAIT THIS TIME
(1) ;OK NOW FALL THRU AND CONTINUE TESTING.....
(1) ;EXIT STAGE LEFT....CHINNG!
8508 007626 017701 172060 MOV @RXCSR,R1 ;ACTUAL
8509 007632 012700 100010 MOV #100010,R0 ;DSC,STD
8510 007636 020001 CMP R0,R1 ;EXPECTED VS ACTUAL
8511 007640 001401 BEQ +4
8512 007642 104001 ERROR 1 ;ONLY DSC & STD SHOULD BE SET
8513 007644 000167 000124 JMP OUT1 ;JUMP AROUND
8514 007650 052777 000010 172034 OUT3: BIS #STD,@RXCSR
8515 ;WAIT FOR CABLE DELAYS
(1) ;*****
(1) ;MODIFY 'HOLD:' ACCORDINGLY FOR FASTER OR SLOWER MACHINE
(1) ;*****
(1) 007656 016702 171236 MOV HOLD,R2 ;SET DELAY TIME
(1) 007662 005302 DEC R2
(1) 007664 001376 BNE -2 ;WAIT THIS TIME
(1) ;OK NOW FALL THRU AND CONTINUE TESTING.....
(1) ;EXIT STAGE LEFT....CHINNG!
8516 007666 017701 172020 MOV @RXCSR,R1 ;ACTUAL
8517 007672 012700 171016 MOV #171016,R0 ;EXPECTED: DSC,RING,CTS,CARDET,DSR,STD,RTS,DTR
8518 007676 020001 CMP R0,R1 ;EXPECTED VS ACTUAL
8519 007700 001401 BEQ +4
8520 007702 104001 ERROR 1 ;CHECK SEC REC JUMPER
8521 007704 042777 000004 172000 BIC #RTS,@RXCSR
8522 ;WAIT FOR CABLE DELAYS

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```

(1)
(1)
(1)
(1) 007712 016702 171202
(1) 007716 005302
(1) 007720 001376
(1)
(1)
8523 007722 017701 171764
8524 007726 012700 131012
8525 007732 020001
8526 007734 001401
8527 007736 104001
8528 007740 042777 000002 171744
8529
(1)
(1)
(1)
(1) 007746 016702 171146
(1) 007752 005302
(1) 007754 001376
(1)
(1)
8530 007756 017701 171730
8531 007762 012700 101010
8532 007766 020001
8533 007770 001401
8534 007772 104001
8535 007774
8536
8537
(1)
(1)
(1)
(5)
(4) 007774 000004
(4)
(3) 007776 052777 000400 171722
(2) 010004 012777 020000 171710
(3) 010012 052777 000400 171706
(2)
(2)
(2) 010020 012777 064001 171700
(2)
(2)
(2) 010026 012777 026026 171666
(1) 010034 032777 004000 171650
(1) 010042 001401
(1) 010044 104004
(1) 010046 052777 000020 171636
(1) 010054 032777 004000 171630
(1) 010062 001001
(1) 010064 104004
(1) 010066 042777 000020 171616
(1)
(1) 010074 032777 004000 171610

```

```

:*****
;MODIFY 'HOLD:'' ACCORDINGLY FOR FASTER OR SLOWER MACHINE
:*****
MOV    HOLD,R2 ;SET DELAY TIME
DEC    R2
BNE    -2      ;WAIT THIS TIME
;OK NOW FALL THRU AND CONTINUE TESTING.....
;EXIT STAGE LEFT....CHINNG!
MOV    @RXCSR,R1 ;ACTUAL
MOV    #131012,R0 ;EXPECTED: DSC,CTS,CARDET,DSR,STD,DTR
CMP    R0,R1    ;EXPECTED VS ACTUAL
BEQ    +4
ERROR  1        ;CHECK H315 CONNECTOR
BIC    #DTR,@RXCSR
;WAIT FOR CABLE DELAYS
:*****
;MODIFY 'HOLD:'' ACCORDINGLY FOR FASTER OR SLOWER MACHINE
:*****
MOV    HOLD,R2 ;SET DELAY TIME
DEC    R2
BNE    -2      ;WAIT THIS TIME
;OK NOW FALL THRU AND CONTINUE TESTING.....
;EXIT STAGE LEFT....CHINNG!
MOV    @RXCSR,R1 ;ACTUAL
MOV    #101010,R0 ;EXPECTED: DSC,DSR,STD
CMP    R0,R1    ;EXPECTED VS ACTUAL
BEQ    +4
ERROR  1        ;CHECK H315 CONNECTOR

OUT1:
::THIS TEST VERIFYS THAT REACT (REC ACTIVE) ASSERTS
::IMMED. WHEN SYNC EXTERNAL MODE IS SELECTED
::AND SYNC SEARCH IS SET
:*****
TST52: SCOPE

BIS    #MRESET,@TXCSR ;MASTER RESET
MOV    #SYNEXT,@PARCSR ;SET THE MODE
BIS    #MRESET,@TXCSR ;MASTER RESET

;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
MOV    #MTDATA!CLK!MINT!BREAK,@TXCSR

;SET MODE ,# OF BITS,PARITY SENSE,&LOAD SYNC REG
MOV    #SYNEXT!EIGHT!NOPAR!26,@PARCSR
BIT    #REACT,@RXCSR
BEQ    +4
ERROR  4        ;REACT SHOULD NOT BE SET
BIS    #SYNSCH,@RXCSR ;SET SYNC SEARCH
BIT    #REACT,@RXCSR
BNE    +4
ERROR  4        ;REACT DID NOT ASSERT
BIC    #SYNSCH,@RXCSR ;DROP SEARCH SYNC

BIT    #REACT,@RXCSR ;IS IT =0?

```



```

(2)
(2)
(2) 010252 012777 030026 171442 ;SET MODE ,# OF BITS,PARIY SENSE,&LOAD SYNC REG
(1) 010260 016703 171432      MOV      #SYNINT!FIVE!NOPAR!26,@PARCSR
(2) 010264 052777 000020 171420  MOV      RXDBUF,R3             ;SET UP FOR ERROR MESSAGE
(2)                    BIS      #SYNSCH,@RXCSR           ;SET SYNC SEARCH
(2)                    ;POKE CLK TO GET RECEIVER INTO SYNCRIOIZATION....
(2) 010272 042777 020000 171426  BIC      #CLK,@TXCSR          ;POKE CLK DOWN
(2) 010300 052777 020000 171420  BIS      #CLK,@TXCSR          ;POKE CLK UP
(2)                    ;POKE CLK TO GET LOGIC INTO SYNCRONIZATION
(2) 010306 042777 020000 171412  BIC      #CLK,@TXCSR          ;POKE CLK DOWN
(2) 010314 052777 020000 171404  BIS      #CLK,@TXCSR          ;POKE CLK UP
(1) 010322 012767 000002 170574  MOV      #2,COUNT
(1) 010330 012767 000005 170564  1$:    MOV      #5,SHIFT           ;# OF SHIFTS
(1) 010336 012767 000026 171134  MOV      #26,$TMP1           ;SYNC CHARACTER
(1) 010344 004767 006554      JSR      PC,RPOKE
(1) 010350 005367 170550      DEC      COUNT
(1) 010354 001403      BEQ      2$
(1)                    ;TEST SYNCNO TO SEE HOW MANY SYNC CHARS WERE SELECTED
(1) 010356 105767 170564      TSTB    SYNCNO
(1) 010362 100762          BMI      1$                  ;TWO SYNC CHARS
(1) 010364 105777 171322  2$:    TSTB    @RXCSR           ;CHECK REC DONE BIT
(1) 010370 100001          BPL      .+4
(1) 010372 104004          ERROR   4                    ;RXDONE SHOULD NOT BE ASSERTED
(1) 010374 032777 004000 171310  BIT      #REACT,@RXCSR
(1) 010402 001001          BNE      .+4
(1) 010404 104004          ERROR   4                    ;REACT SHOULD BE ASSERTED
(1) 010406 012767 000005 170506  MOV      #5,SHIFT
(1) 010414 012767 000021 171056  MOV      #21,$TMP1           ;ANY CHARACTER
(1) 010422 004767 006476      JSR      PC,RPOKE
(1) 010426 105777 171260      TSTB    @RXCSR           ;CHECK RXDONE
(1) 010432 100401          BMI      .+4
(1) 010434 104004          ERROR   4                    ;RXDONE SHOULD BE ASSERTED
(1) 010436 032777 004000 171246  BIT      #REACT,@RXCSR
(1) 010444 001001          BNE      .+4
(1) 010446 104004          ERROR   4                    ;REACT SHOULD STILL BE ASSERTED
(1) 010450 042777 000020 171234  BIC      #SYNSCH,@RXCSR       ;CLR SYNC SEARCH
(1) 010456 032777 004000 171226  BIT      #REACT,@RXCSR       ;IT SHOULD DROP IMMEDIATELY
(1) 010464 001401          BEQ      .+4
(1) 010466 104004          ERROR   4                    ;REACT SHOULD BE CLR
(1) 010470 105777 171216      TSTB    @RXCSR           ;RXDONE
(1) 010474 100401          BMI      .+4
(1) 010476 104004          ERROR   4                    ;RXDONE SHOULD STILL BE ASSERTED
(1) 010500 012700 000021      MOV      #21,R0             ;EXPECTED DATA
(1) 010504 017701 171206      MOV      @RXDBUF,R1          ;ACTUAL DATA
(1) 010510 020001          CMP      R0,R1             ;COMPARE EXP VS ACT
(1) 010512 001401          BEQ      .+4
(1) 010514 104002          ERROR   2                    ;DATA CHARS SHOULD COMPARE
(1) 010516 105777 171170      TSTB    @RXCSR           ;CHECK RXDONE
(1) 010522 100001          BPL      .+4
(1) 010524 104004          ERROR   4                    ;RXDONE SHOULD BE CLR FROM
(1)                    ;PREVIOUS READING OF RXDBUF
(1)
8540
(1)                    ;;VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING
(1)                    ;;IN TWO * SYNC CHARS THRU MAINT DATA BIT
(1)                    ;;WATCH THE REACT BIT
(1)                    ;;ON THE THIRD * CHARACTER IT SHOULD SET RXDONE

```

```

(1)                                     ::*: DEPENDENT ON MONITOR.....
(1)                                     ::IF ONE SYNC STRAP IS SELECTED THEN IT WILL ONLY
(1)                                     ::TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT
(1)                                     ::ON THE SECOND CHARACTER
(1)                                     ::ALSO CHECK THIS CHARACTER IN RXDBUF
(1)                                     ::AND CHECK OPERATION OF SYNSCH
(1)                                     ::MODE: SYNC INTERNAL
(1)                                     ::LENGTH: SIX
(1)                                     :
(5) *****
(4) 010526 000004 TST55: SCOPE
(4)
(3) 010530 052777 000400 171170     BIS      #MRESET,@TXCSR ;MASTER RESET
(2) 010536 012777 030000 171156     MOV      #SYNINT,@PARCSR ;SET THE MODE
(3) 010544 052777 000400 171154     BIS      #MRESET,@TXCSR ;MASTER RESET
(2)
(2)                                     ;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
(2) 010552 012777 064001 171146     MOV      #MTDATA!CLK!MINT!BREAK,@TXCSR
(2)
(2)                                     ;SET MODE ,# OF BITS,PARITY SENSE,&LOAD SYNC REG
(2) 010560 012777 032026 171134     MOV      #SYNINT!SIX!NOPAR!26,@PARCSR
(1) 010566 016703 171124             MOV      RXDBUF,R3       ;SET UP FOR ERROR MESSAGE
(2) 010572 052777 000020 171112     BIS      #SYNSCH,@RXCSR  ;SET SYNC SEARCH
(2)                                     ;POKE CLK TO GET RECEIVER INTO SYNCROIZATION....
(2) 010600 042777 020000 171120     BIC      #CLK,@TXCSR     ;POKE CLK DOWN
(2) 010606 052777 020000 171112     BIS      #CLK,@TXCSR     ;POKE CLK UP
(2)                                     ;POKE CLK TO GET LOGIC INTO SYNCRONIZATION
(2) 010614 042777 020000 171104     BIC      #CLK,@TXCSR     ;POKE CLK DOWN
(2) 010622 052777 020000 171076     BIS      #CLK,@TXCSR     ;POKE CLK UP
(1) 010630 012767 000002 170266     MOV      #2,COUNT
(1) 010636 012767 000006 170256     1$:     MOV      #6,SHIFT      ;# OF SHIFTS
(1) 010644 012767 000026 170626     MOV      #26,$TMP1      ;SYNC CHARACTER
(1) 010652 004767 006246             JSR      PC,RPOKE
(1) 010656 005367 170242             DEC      COUNT
(1) 010662 001403             BEQ      2$
(1)                                     ;TEST SYNCNO TO SEE HOW MANY SYNC CHARS WERE SELECTED
(1) 010664 105767 170256             TSTB     SYNCNO
(1) 010670 100762             BMI      1$             ;TWO SYNC CHARS
(1) 010672 105777 171014     2$:     TSTB     @RXCSR        ;CHECK REC DONE BIT
(1) 010676 100001             BPL      .+4
(1) 010700 104004             ERROR   4              ;RXDONE SHOULD NOT BE ASSERTED
(1) 010702 032777 004000 171002     BIT      #REACT,@RXCSR
(1) 010710 001001             BNE     .+4
(1) 010712 104004             ERROR   4              ;REACT SHOULD BE ASSERTED
(1) 010714 012767 000006 170200     MOV      #6,SHIFT
(1) 010722 012767 000021 170550     MOV      #21,$TMP1      ;ANY CHARACTER
(1) 010730 004767 006170             JSR      PC,RPOKE
(1) 010734 105777 170752             TSTB     @RXCSR        ;CHECK RXDONE
(1) 010740 100401             BMI     .+4
(1) 010742 104004             ERROR   4              ;RXDONE SHOULD BE ASSERTED
(1) 010744 032777 004000 170740     BIT      #REACT,@RXCSR
(1) 010752 001001             BNE     .+4
(1) 010754 104004             ERROR   4              ;REACT SHOULD STILL BE ASSERTED
(1) 010756 042777 000020 170726     BIC      #SYNSCH,@RXCSR ;CLR SYNC SEARCH
(1) 010764 032777 004000 170720     BIT      #REACT,@RXCSR ;IT SHOULD DROP IMMEDIATELY
(1) 010772 001401             BEQ      .+4

```

CNDUQ-AO
CNDUQA.M11

MACY11 30(1046)
30-OCT-82 12:11

14-DEC-82 09:56 PAGE 62-40
INITIALIZE THE COMMON TAGS

SEQ 0054

```
(1) 010774 104004  
(1) 010776 105777 170710  
(1) 011002 100401  
(1) 011004 104004  
(1) 011006 012700 000021  
(1) 011012 017701 170700  
(1) 011016 020001  
(1) 011020 001401  
(1) 011022 104002  
(1) 011024 105777 170662  
(1) 011030 100001  
(1) 011032 104004  
(1)  
(1)  
8541  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
(1)  
(5)  
(4) 011034 000004  
(4)  
(3) 011036 052777 000400 170662  
(2) 011044 012777 030000 170650  
(3) 011052 052777 000400 170646  
(2)  
(2)  
(2) 011060 012777 064001 170640  
(2)  
(2)  
(2) 011066 012777 034026 170626  
(1) 011074 016703 170616  
(2) 011100 052777 000020 170604  
(2)  
(2) 011106 042777 020000 170612  
(2) 011114 052777 020000 170604  
(2)  
(2) 011122 042777 020000 170576  
(2) 011130 052777 020000 170570  
(1) 011136 012767 000002 167760  
(1) 011144 012767 000007 167750  
(1) 011152 012767 000026 170320  
(1) 011160 004767 005740  
(1) 011164 005367 167734  
(1) 011170 001403  
(1)  
(1) 011172 105767 167750  
(1) 011176 100762
```

```
ERROR 4 ;REACT SHOULD BE CLR  
TSTB @RXCSR ;RXDONE  
BMI .+4  
ERROR 4 ;RXDONE SHOULD STILL BE ASSERTED  
MOV #21,R0 ;EXPECTED DATA  
MOV @RXDBUF,R1 ;ACTUAL DATA  
CMP R0,R1 ;COMPARE EXP VS ACT  
BEQ .+4  
ERROR 2 ;DATA CHARS SHOULD COMPARE  
TSTB @RXCSR ;CHECK RXDONE  
BPL .+4  
ERROR 4 ;RXDONE SHOULD BE CLR FROM  
 ;PREVIOUS READING OF RXDBUF
```

```
::VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING  
::IN TWO * SYNC CHARS THRU MAINT DATA BIT  
::WATCH THE REACT BIT  
::ON THE THIRD * CHARACTER IT SHOULD SET RXDONE  
::*: DEPENDENT ON MONITOR.....  
::IF ONE SYNC STRAP IS SELECTED THEN IT WILL ONLY  
::TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT  
::ON THE SECOND CHARACTER  
::ALSO CHECK THIS CHARACTER IN RXDBUF  
::AND CHECK OPERATION OF SYN SCH  
::MODE: SYNC INTERNAL  
::LENGTH:SEVEN
```

TST56: SCOPE

```
BIS #MRESET,@TXCSR ;MASTER RESET  
MOV #SYNINT,@PARCSR ;SET THE MODE  
BIS #MRESET,@TXCSR ;MASTER RESET  
  
;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE  
MOV #MCDATA!CLK!MINT!BREAK,@TXCSR  
  
;SET MODE ,# OF BITS,PARITY SENSE,&LOAD SYNC REG  
MOV #SYNINT!SEVEN!NOPAR!26,@PARCSR  
MOV RXDBUF,R3 ;SET UP FOR ERROR MESSAGE  
BIS #SYNSCH,@RXCSR ;SET SYNC SEARCH  
;POKE CLK TO GET RECEIVER INTO SYNCROIZATION....  
BIC #CLK,@TXCSR ;POKE CLK DOWN  
BIS #CLK,@TXCSR ;POKE CLK UP  
;POKE CLK TO GET LOGIC INTO SYNCHRONIZATION  
BIC #CLK,@TXCSR ;POKE CLK DOWN  
BIS #CLK,@TXCSR ;POKE CLK UP  
1$: MOV #2,COUNT  
MOV #7,SHIFT ;# OF SHIFTS  
MOV #26,$TMP1 ;SYNC CHARACTER  
JSR PC,RPOKE  
DEC COUNT  
BEQ 2$  
;TEST SYNCNO TO SEE HOW MANY SYNC CHARS WERE SELECTED  
TSTB SYNCNO  
BMI 1$ ;TWO SYNC CHARS
```



```
(1)      ;;CHAR:12
(1)      ;;
(5)      *****
(4) 012076 000004      TST61: SCOPE
(4)
(3) 012100 052777 000400 167620      BIS      #MRESET,@TXCSR ;MASTER RESET
(2) 012106 012777 000000 167606      MOV      #ISYMOD,@PARCSR ;SET THE MODE
(3) 012114 052777 000400 167604      BIS      #MRESET,@TXCSR ;MASTER RESET
(2)
(2) 012122 012777 064001 167576      ;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
(2)      MOV      #MTDATA!CLK!MINT!BREAK,@TXCSR
(2)
(2) 012130 012777 000000 167564      ;SET MODE ,# OF BITS,PARITY SENSE,&LOAD SYNC REG
(2) 012136 052777 000020 167546      MOV      #ISYMOD!FIVE!NOPAR!0,@PARCSR
(2)      BIS      #SYNSCH,@RXCSR ;SET SYNC SEARCH
(2)      ;POKE CLK TO GET RECEIVER INTO SYNCROIZATION....
(2) 012144 042777 020000 167554      BIC      #CLK,@TXCSR ;POKE CLK DOWN
(2) 012152 052777 020000 167546      BIS      #CLK,@TXCSR ;POKE CLK UP
(2)      ;POKE CLK TO GET LOGIC INTO SYNCHRONIZATION
(2) 012160 042777 020000 167540      BIC      #CLK,@TXCSR ;POKE CLK DOWN
(2) 012166 052777 020000 167532      BIS      #CLK,@TXCSR ;POKE CLK UP
(1) 012174 016703 167516      MOV      RXDBUF,R3 ;SET UP FOR ERROR MESSAGE
(1) 012200 012700 000012      MOV      #12,R0 ;EXPECTED
(1) 012204 012767 000007 166710      MOV      #7,SHIFT ;# OF SHIFTS
(1) 012212 012767 000124 167260      MOV      #124,$TMP1 ;DATA CHAR
(1) 012220 004767 004700      JSR      PC,RPOKE ;SHIFT IN THIS CHAR
(1) 012224 105777 167462      TSTB    @RXCSR ;RXDONE ?
(1) 012230 100401      BMI     .+4
(1) 012232 104004      ERROR   4 ;RXDONE SHOULD BE SET
(1) 012234 017701 167456      MOV     @RXDBUF,R1 ;ACTUAL
(1) 012240 020001      CMP     R0,R1 ;COMPARE EXPECTED VS. ACTUAL
(1) 012242 001401      BEQ    .+4
(1) 012244 104002      ERROR   2 ;RECEIVED DATA DID NOT MATCH
(1)      ;EXPECTED DATA - CHECK MAINT DATA
(1)      ;OR RECEIVER LOGIC
(1) 012246 012767 000007 166646      MOV     #7,SHIFT ;# OF SHIFTS
(1) 012254 012767 000124 167216      MOV     #124,$TMP1 ;DATA CHAR
(1) 012262 004767 004636      JSR     PC,RPOKE ;SHIFT IN THIS CHAR
(1)      ;NOW SHIFT IN A SECOND CHARACTER WITHOUT READING RXDBUF
(1) 012266 012767 000007 166626      MOV     #7,SHIFT ;# OF SHIFTS
(1) 012274 012767 000124 167176      MOV     #124,$TMP1 ;DATA CHAR
(1) 012302 004767 004616      JSR     PC,RPOKE ;SHIFT IN THIS CHAR
(1) 012306 012700 140012      MOV     #140000!12,R0 ;EXPECTED DATA PLUS
(1)      ;RXERR & OVRRUN
(1) 012312 017701 167400      MOV     @RXDBUF,R1 ;ACTUAL
(1) 012316 020001      CMP     R0,R1 ;COMPARE EXP VS. ACT
(1) 012320 001401      BEQ    .+4
(1) 012322 104002      ERROR   2 ;SPECIFICALLY LOOK AT RXERR &
(1)      ;OVRRUN BITS...THEY BOTH SHOULD BE SET
(1)
8545
8546
(2)
(2)
(2)
(2)
;END OF PASS
;TYPE NAME OF TEST
;UPDATE PASS COUNT
;CHECK FOR EXIT TO ACT-11
```



```

(2) ;HORIZONTAL TAB PROCESSOR
(2)
(2) 013230 112716 000040 8$: MOV B #',(SP) ;:REPLACE TAB WITH SPACE
(2) 013234 004767 000014 9$: JSR PC,$TYPEC ;:TYPE A SPACE
(2) 013240 132767 000007 000052 BIT B #7,$CHARCNT ;:BRANCH IF NOT AT
(2) 013246 001372 BNE 9$ ;:TAB STOP
(2) 013250 005726 TST (SP)+ ;:POP SPACE OFF STACK
(2) 013252 000724 BR 2$ ;:GET NEXT CHARACTER
(2) 013254 105777 166170 $TYPEC: TST B @$TSPS ;:WAIT UNTIL PRINTER IS READY
(2) 013260 100375 BPL $TYPEC
(2) 013262 116677 000002 166162 MOV B 2(SP),@$TPB ;:LOAD CHAR TO BE TYPED INTO DATA REG.
(2)
(2) 013270 122766 000015 000002 CMP B #CR,2(SP) ;:IS CHARACTER A CARRIAGE RETURN?
(2) 013276 001003 BNE 1$ ;:BRANCH IF NO
(2) 013300 105067 000014 CLR B $CHARCNT ;:YES--CLEAR CHARACTER COUNT
(2) 013304 000406 BR $TYPEX ;:EXIT
(2) 013306 122766 000012 000002 1$: CMP B #LF,2(SP) ;:IS CHARACTER A LINE FEED?
(2) 013314 001402 BEQ $TYPEX ;:BRANCH IF YES
(2) 013316 105227 INCB (PC)+ ;:COUNT THE CHARACTER
(2) 013320 000000 $CHARCNT: .WORD 0 ;:CHARACTER COUNT STORAGE
(2) 013322 000207 $TYPEX: RTS PC
(2)
(2)
(2)
(2) ;ASCII STRING INPUT ROUTINE
(2)
(2) 013324 017667 000000 000014 .INSTR: MOV @(SP),.MSG ;:PICK UP MESSAGE
(2) 013332 062716 000002 ADD #2,(SP) ;:JUMP AROUND MESSAGE FOR RTI
(2) 013336 105767 166204 TST B $ENV ;:APT CONTROL
(2) 013342 001036 BNE INSTR2 ;:YES NO TYPE
(2) 013344 104401 .INST1: TYPE
(2) 013346 000000 .MSG: 0
(2) 013350 012704 016124 MOV #INBUF,R4 ;:GET STARTING LOC OF INBUF
(2) 013354 012703 000007 MOV #7,R3 ;:MAX # OF CHARS
(2) 013360 105777 166060 1$: TST B @$TKS ;TTY FLAG
(2) 013364 100375 BPL 1$
(2) 013366 117714 166054 MOV B @$TKB,(R4) ;:TAKE CHAR
(2) 013372 142714 000200 BIC B #200,(R4) ;:STRIP
(2) 013376 121427 000025 CMP B (R4),#25 ;:IS IT <^G>
(2) 013402 001760 BEQ .INST1
(2) 013404 122427 000015 CMP B (R4)+,#15 ;:CHECK FOR CR
(2) 013410 001413 BEQ INSTR2
(2) 013412 105777 166032 2$: TST B @$TSPS ;:TEST FLAG
(2) 013416 100375 BPL 2$
(2) 013420 117777 166022 166024 MOV B @$TKB,$$TPB ;:ECHO CHARACTER
(2) 013426 005303 DEC R3 ;:DID YOU TYPE TOO MANY CHARS ?
(2) 013430 001353 BNE 1$
(2) 013432 104401 .INSTE: TYPE
(2) 013434 015410 MQM ;?
(2) 013436 000742 BR .INST1 ;:RETRY
(2) 013440 000002 INSTR2: RTI
(2)
(2) ;CONVERT ASCII STRING TO OCTAL
(2)
(2) 013442 011605 .PARAM: MOV (SP),R5 ;:PUT CONTENTS OF SP INTO R5

```



```
(2) 014100 001325                BNE 1$      ;DO THIS ROUTINE AGAIN IF NOT EQUAL TO 0
(2) 014102 000002                RTI       ;RETURN TO PROGRAM
(2) 014104 000000                WRDCNT: 0
(2) 014106 000000                CHRCNT: 0
(2)             014107                SPACNT=CHRCNT+1
(2) 014110 000000                BINWRD: 0
(2)
(2)                               ;COMPARE THE FIRST CHARACTER IN THE TELETYPE INPUT
(2)                               ;BUFFER TO THE CHARACTERS 'N' AND 'Y'
(2)                               ;IF THE CHARACTER IS 'N' CLEAR THE FLAG
(2)                               ;IF THE CHARACTER IS 'Y' SET THE FLAG
(2)
(2) 014112 017605 000000          .SETFLG:MOV @ (SP),R5
(2) 014116 122767 000116 002000  CMPB #'N,INBUF ;IS IT 'N' ?
(2) 014124 001002                BNE 1$
(2) 014126 105015                CLRB (R5)     ;000
(2) 014130 000406                BR 2$
(2) 014132 122767 000131 001764 1$: CMPB #'Y,INBUF ;IS IT 'Y' ?
(2) 014140 001005                BNE 3$
(2) 014142 112715 177777          MOVB #-1,(R5) ;377
(2) 014146 062716 000002          2$: ADD #2,(SP)
(2) 014152 000002                RTI
(2) 014154 104407                3$: INSTER ;RETRY
(2) 014156 000755                BR .SETFLG
(2)                               .SBTTL ERROR HANDLER ROUTINE
(2)
(2)
(3) *****
(2) *THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,
(2) *SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL
(2) *AND GO TO SAVIT ON ERROR
(2) *THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
(2) *SW15=1 HALT ON ERROR
(2) *SW13=1 INHIBIT ERROR TYPEOUTS
(2) *SW10=1 BELL ON ERROR
(2) *SW09=1 LOOP ON ERROR
(2) *CALL
(2) * ERROR N ;:ERROR=EMT AND N=ERROR ITEM NUMBER
(2)
(2) 014160          $ERROR:
(2) 014160 105267 165217          7$: INCB $ERFLG ;:SET THE ERROR FLAG
(2) 014164 001775                BEQ 7$ ;:DON'T LET THE FLAG GO TO ZERO
(2) 014166 016777 165210 165246  MOV $STNM,@DISPLAY ;:DISPLAY TEST NUMBER AND ERROR FLAG
(2) 014174 032777 002670 165236  BIT #BIT10,@SWR ;:BELL ON ERROR?
(2) 014202 001402                BEQ 1$ ;:NO - SKIP
(2) 014204 104401 001516          TYPE ,SBELL ;:RING BELL
(2) 014210 005267 165176          1$: INC $ERTTL ;:COUNT THE NUMBER OF ERRORS
(2) 014214 011667 165176          MOV (SP),$ERRPC ;:GET ADDRESS OF ERROR INSTRUCTION
(2) 014220 162767 000002 165170  SUB #2,$ERRPC
(2) 014226 117767 165164 165160  MOVB @$ERRPC,$ITEMB ;:STRIP AND SAVE THE ERROR ITEM CODE
(2) 014234 032777 020000 165176  BIT #BIT13,@SWR ;:SKIP TYPEOUT IF SET
(2) 014242 001004                BNE 20$ ;:SKIP TYPEOUTS
(2) 014244 004767 000072          JSR PC,SAVIT ;:GO TO USER ERROR ROUTINE
(2) 014250 104401 001523          TYPE ,$CRLF
(2) 014254          20$:
(2) 014254 122767 000001 165264  CMPB #APTENV,$ENV ;:RUNNING IN APT MODE
(2) 014262 001007                BNE 2$ ;:NO,SKIP APT ERROR REPORT
```



```

(2) 015024 012605     MOV      (SP)+,R5          ;RESTORE R0-R5
(2) 015026 012604     MOV      (SP)+,R4
(2) 015030 012603     MOV      (SP)+,R3
(2) 015032 012602     MOV      (SP)+,R2
(2) 015034 012601     MOV      (SP)+,R1
(2) 015036 012600     MOV      (SP)+,R0
(2) 015040 012767 014762 162756  MOV      #,PFAIL,24      ;SET UP FOR POWER FAILURE
(2) 015046 106427 000300  MTPS     #300
(2) 015052 012706 001100  MOV      #STACK,SP
(2) 015056 005067 001104  CLR      TEMP
(2) 015062 005267 001100  INC      TEMP
(2) 015066 001375     BNE     .-4
(2) 015070 104413     CONVRT
(2) 015072 015114     PFTAB
(2) 015074 104401     TYPE
(2) 015076 015417     MPFAIL
(2) 015100 005067 164277  CLR      $ERFLG
(2) 015104 005067 164306  CLR      $ERRPC
(2) 015110 000177 163770  JMP      @RETURN
(2) 015114 000001     PFTAB:  1
(2) 015116 006 002     .BYTE  6,2
(2) 015120 000207     RETURN
(2) 015122 005015 041412 042116  MTITLE: .ASCIZ <15><12><12>/CNDUQ-AO DUV11 TAPE A /<15><12>
(2) 015130 050525 040455 020060
(2) 015136 052504 030526 020061
(2) 015144 040524 042520 040440
(2) 015152 006440 000012
(2) 015156 005015 042526 020103  MVECTO: .ASCIZ <15><12>/VEC ADD-/
(2) 015164 042101 026504 000
(2) 015171 015 030412 052123  MREGAD: .ASCIZ <15><12>/1ST DEV: REC CSR ADD-/
(2) 015176 042040 053105 020072
(2) 015204 042522 020103 051503
(2) 015212 020122 042101 026504
(2) 015220 000
(2) 015221 015 046412 046125  MMULT:  .ASCIZ <15><12>/MULT DEV ? (Y OR N)-/
(2) 015226 020124 042504 020126
(2) 015234 020077 054450 047440
(2) 015242 020122 024516 000055
(2) 015250 005015 040514 052123  MLASTD: .ASCIZ <15><12>/LAST DEV: REC CSR ADDR-/
(2) 015256 042040 053105 020072
(2) 015264 042522 020103 051503
(2) 015272 020122 042101 051104
(2) 015300 000055
(2) 015302 042075 053105 041511  DEVICE: .ASCIZ /=DEVICE /
(2) 015310 020105 000040
(2) 015314 005015 042523 042514  MCOV:   .ASCIZ <15><12>/SELECT TO RUN @ACTREG/
(2) 015322 052103 052040 020117
(2) 015330 052522 020116 040500
(2) 015336 052103 042522 000107
(2) 015344 005015 053117 046106  MRANGE: .ASCIZ <15><12>/OVFLO:RETYPE LAST DEV RXCSR ADDS-/
(2) 015352 035117 042522 054524
(2) 015360 042520 046040 051501
(2) 015366 020124 042504 020126
(2) 015374 054122 051503 020122
(2) 015402 042101 051504 000055
(2) 015410 020040 000077  MQM:    .ASCIZ / ?/

```



```

(2) 016076 000040
(2) 016100 051440 051127 020075 MMSWR: .ASCIZ / SWR= /
(2) 016106 020040 000
(2) 016111 040 020040 042516 MMNEW: .ASCIZ / NEW= /
(2) 016116 036527 020040 000
(2) 016124 .EVEN
(2)
(2) ;BUFFERS FOR INPUT-OUTPUT
(2)
(2) 016124 000000 INBUF: 0
(2) .+.40
(2) 016166 000000 TEMP: 0
(2) .+.40
(2) 016230 000000 MDATA: 0
(2) .+.40
(3) .SBTTL SCOPE HANDLER ROUTINESTARS
(3) ;*THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
(3) ;*AND LOAD THE TEST NUMBER($TSTNM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
(3) ;*AND LOAD THE ERROR FLAG ($ERFLG) INTO DISPLAY<15:08>
(3) ;*THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
(3) ;*SW14=1 LOOP ON TEST
(3) ;*SW11=1 INHIBIT ITERATIONS
(3) ;*SW09=1 LOOP ON ERROR
(3) ;*SW08=1 LOOP ON TEST IN SWR<7:0>
(3) ;*CALL
(3) ;* SCOPE ;;SCOPE=IOT
(3) 016272 $SCOPE:
(5) ;SCOPE LOOP AND INTERATION HANDLER
(5)
(5) .SCOPE:
(5) 016272 004767 174374 JSR PC,CKSWR
(5) 016276 005067 163114 CLR $ERRPC ;CLEAR LAST ERROR PC
(5) 016302 022716 003376 CMP #TST1+2,(SP) ;IS SCOPE AT BEGINING OF TEST 1?
(5) 016306 001422 BEQ $XTSTR ;YES NO LOOP.
(5)
(5) 016310 032777 040000 163122 TTST: BIT #BIT14,@SWR ;THIS CODE IS FOR TESTING FOR BIT 14
(5) 016316 001412 BEQ 1$ ;ON LSI WHICH SYSMAC CANNOT HANDLE
(5) 016320 016767 163056 163060 MOV $TSTNM,$LPADR
(5) 016326 000406 BR 1$
(5) 016330 105777 163110 TSTB @STKS ;KEYBOARD DONE?
(5) 016334 100123 BPL $OVER ;BR IF NO
(5) 016336 017766 163104 177776 MOV @STKB,-2(SP) ;CLEAR DONE BIT
(3) 016344 032777 040000 163066 1$: BIT #BIT14,@SWR ;LOOP ON PRESENT TEST?
(3) 016352 001114 BNE $OVER ;YES IF SW14=1
(3) ;*****START OF CODE FOR THE XOR TESTER*****
(3) 016354 000416 $XTSTR: BR 6$ ;IF RUNNING ON THE 'XOR' TESTER CHANGE
(3) ;THIS INSTRUCTION TO A 'NOP' (NOP=240)
(3) 016356 013746 000004 MOV @#ERRVEC,-(SP) ;SAVE THE CONTENTS OF THE ERROR VECTOR
(3) 016362 012737 016402 000004 MOV #5$,@#ERRVEC ;SET FOR TIMEOUT
(3) 016370 005737 177060 TST @#177060 ;TIME OUT ON XOR?
(3) 016374 012637 000004 MOV (SP)+,@#ERRVEC ;RESTORE THE ERROR VECTOR
(3) 016400 000463 BR $SVLAD ;GO TO THE NEXT TEST
(3) 016402 022626 5$: CMP (SP)+,(SP)+ ;CLEAR THE STACK AFTER A TIME OUT
(3) 016404 012637 000004 MOV (SP)+,@#ERRVEC ;RESTORE THE ERROR VECTOR

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(3) 016410 000423        BR      7$           ;;LOOP ON THE PRESENT TEST
(3) 016412               6$:;#####END OF CODE FOR THE XOR TESTER#####
(3) 016412 032777 000400 163020 BIT      #BIT08,@SWR      ;;LOOP ON SPEC. TEST?
(3) 016420 001404        BEQ      2$           ;;BR IF NO
(3) 016422 127767 163012 162752 CMPB    @SWR,$STNM     ;;ON THE RIGHT TEST?   SWR<7:0>
(3) 016430 001465        BEQ      $OVER       ;;BR IF YES
(3) 016432 105767 162745 2$:      TSTB    $ERFLG      ;;HAS AN ERROR OCCURRED?
(3) 016436 001421        BEQ      3$           ;;BR IF NO
(3) 016440 126767 162751 162735 CMPB    $ERMAX,$ERFLG ;;MAX. ERRORS FOR THIS TEST OCCURRED?
(3) 016446 101015        BHI      3$           ;;BR IF NO
(3) 016450 032777 001000 162762 BIT      #BIT09,@SWR      ;;LOOP ON ERROR?
(3) 016456 001404        BEQ      4$           ;;BR IF NO
(3) 016460 016767 162724 162720 7$:   MOV     $LPERR,$LPADR  ;;SET LOOP ADDRESS TO LAST SCOPE
(3) 016466 000446        BR      $OVER
(3) 016470 105067 162707 4$:      CLRB    $ERFLG      ;;ZERO THE ERROR FLAG
(3) 016474 005067 163012      CLR     $TIMES      ;;CLEAR THE NUMBER OF ITERATIONS TO MAKE
(3) 016500 000415        BR      1$           ;;ESCAPE TO THE NEXT TEST
(3) 016502 032777 004000 162730 3$:   BIT      #BIT11,@SWR     ;;INHIBIT ITERATIONS?
(3) 016510 001011        BNE      1$           ;;BR IF YES
(3) 016512 005767 163016      TST     $PASS       ;;IF FIRST PASS OF PROGRAM
(3) 016516 001406        BEQ      1$           ;;           INHIBIT ITERATIONS
(3) 016520 005267 162660      INC     $ICNT       ;;INCREMENT ITERATION COUNT
(3) 016524 026767 162762 162652 CMP     $TIMES,$ICNT   ;;CHECK THE NUMBER OF ITERATIONS MADE
(3) 016532 002024        BGE      $OVER       ;;BR IF MORE ITERATION REQUIRED
(3) 016534 012767 000001 162642 1$:   MOV     #1,$ICNT     ;;REINITIALIZE THE ITERATION COUNTER
(3) 016542 016767 000056 162742      MOV     $MXCNT,$TIMES ;;SET NUMBER OF ITERATIONS TO DO
(3) 016550 105267 162626      $SVLAD: INCB    $STNM      ;;COUNT TEST NUMBERS
(3) 016554 116767 162622 162750 MOVB    $STNM,$STEN   ;;SET TEST NUMBER IN APT MAILBOX
(3) 016562 011667 162620      MOV     (SP),$LPADR  ;;SAVE SCOPE LOOP ADDRESS
(3) 016566 011667 162616      MOV     (SP),$LPERR  ;;SAVE ERROR LOOP ADDRESS
(3) 016572 005067 162716      CLR     $ESCAPE     ;;CLEAR THE ESCAPE FROM ERROR ADDRESS
(3) 016576 112767 000001 162611 MOVB    #1,$ERMAX    ;;ONLY ALLOW ONE(1) ERROR ON NEXT TEST
(3) 016604 016777 162572 162630 $OVER:  MOV     $STNM,@DISPLAY ;;DISPLAY TEST NUMBER
(3) 016612 016716 162570      MOV     $LPADR,(SP)  ;;FUDGE RETURN ADDRESS
(5) 016616 000002        4$:      RTI
(5) 016620 001407        BRW:    1407
(5) 016622 000432        BRX:    432
(3) 016624 000005        $MXCNT: 5           ;;MAX. NUMBER OF ITERATIONS
(2)               .SBTTL TRAP DECODER
(2)
(3)               ;:*****
(2)               ;:*THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
(2)               ;:*AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
(2)               ;:*OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
(2)               ;:*GO TO THAT ROUTINE.
(2)
(2) 016626 010046      $TRAP: MOV     R0,-(SP)   ;;SAVE R0
(2) 016630 016600 000002 MOV     2(SP),R0     ;;GET TRAP ADDRESS
(2) 016634 005740      TST     -(R0)       ;;BACKUP BY 2
(2) 016636 111000      MOVB    (R0),R0     ;;GET RIGHT BYTE OF TRAP
(2) 016640 006300      ASL     R0          ;;POSITION FOR INDEXING
(2) 016642 016000 016662 MOV     $TRPAD(R0),R0 ;;INDEX TO TABLE
(2) 016646 000200      RTS     R0         ;;GO TO ROUTINE
(2)
(2)
(2)               ;:THIS IS USE TO HANDLE THE "GETPRI" MACRO

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8632      ;STMP1 NOW HAS EVEN PARITY CHARACTER
8633      017360 000207       3$:      RTS      PC
8634      017362 062716 000002 TRPREG: ADD      #2,(SP) ;ALLOW IT TO "CRUNCH" INTO ERROR BACK
8635      ;IN MAIN PART OF THE PROGRAM
8636      017366 000002      RTI
8637      017370          POINT=.          ;SAVE POINTER
(1)      000100 000100          .=100
(1)      000102 000300          $CLKVEC          ;LKVEC HANDLER
(1)      000140 000140          300          ;INTERRUPT HANDLER PRI
(1)      000142 170000          .=140          ;BRKVEC
(1)      000144 170000          170000          ;ODT START ADDRESS
(1)      000146 000300          300          ;PRIORITY
(1)      017370 017370          .=POINT          ;RESTORE POINTER
(1)      017374 104401 017376          $CLKVEC:          TYPE,CLKMES
(1)      017376 000000          HALT
(1)      017378 005015 045514 042526          CLKMES: .ASCIZ <15><12>/LKVEC INTERRUPT - DISCONNECT LTC /
(1)      017404 020103 047111 042524
(1)      017412 051122 050125 020124
(1)      017420 020055 044504 041523
(1)      017426 047117 042516 052103
(1)      017434 046040 041524 000040
8638      000001      .END

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CNDUQ-A0
CNDUQA.M11

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CROSS REFERENCE TABLE -- USER SYMBOLS

L 6

SEQ 0076

AAA	003200	8165#	
ABASE =	000000	8165	
ACDW1 =	000000	8165	
ACDW2 =	000000	8165	
ACPUOP=	000000	8165	
ACTREG	001166	8165#*	8546
ADDW0 =	000000	8165	
ADDW1 =	000000	8165	
ADDW10=	000000	8165	
ADDW11=	000000	8165	
ADDW12=	000000	8165	
ADDW13=	000000	8165	
ADDW14=	000000	8165	
ADDW15=	000000	8165	
ADDW2 =	000000	8165	
ADDW3 =	000000	8165	
ADDW4 =	000000	8165	
ADDW5 =	000000	8165	
ADDW6 =	000000	8165	
ADDW7 =	000000	8165	
ADDW8 =	000000	8165	
ADDW9 =	000000	8165	
ADEVCT=	000000	8165	
ADEVM =	000000	8165	
ADRCNT=	013641	8546#*	
AENV =	000000	8165	
AENVM =	000000	8165	
AFATAL=	000000	8165	
AMADR1=	000000	8165	
AMADR2=	000000	8165	
AMADR3=	000000	8165	
AMADR4=	000000	8165	
AMAMS1=	000000	8165	
AMAMS2=	000000	8165	
AMAMS3=	000000	8165	
AMAMS4=	000000	8165	
AMSGAD=	000000	8165	
AMSLG=	000000	8165	
AMSGTY=	000000	8165	
AMTYP1=	000000	8165	
AMTYP2=	000000	8165	
AMTYP3=	000000	8165	
AMTYP4=	000000	8165	
APASS =	000000	8165	
APRIOR=	000000	8165	
APTCSU=	000040	7023#	8546
APTENV=	000001	7023#	8546
APTSIZ=	000200	7023#	8165
APTSPD=	000100	7023#	8546
ASWREG=	000000	8165	
ATESTN=	000000	8165	
AUNIT =	000000	8165	
AUSWR =	000000	8165	
AVECT1=	C00000	8165	
AVECT2=	000000	8165	
BASEAD	001154	8165#*	8546*

\$DDW4	001622	8165#		
\$DDW5	001624	8165#		
\$DDW6	001626	8165#		
\$DDW7	001630	8165#		
\$DDW8	001632	8165#		
\$DDW9	001634	8165#		
\$DEVCT	001536	8165#		
\$DEVM	001604	8165#		
\$E	= 000002	6851#		
\$ENDAD	012644	8165	8546#	
\$ENV	001546	7023	8165#	8546
\$ENVM	001547	7023	8165#	8546
\$ERFLG	001403	8165#*	8546*	
\$ERMAX	001415	8165#*	8546*	
\$ERROR	014160	8165	8546#	
\$ERRPC	001416	8165#*	8546*	
\$ERRTB	001652	8165#	8546	
\$ERRTY	014400	8546#		
\$ERTTL	001412	8165#*	8546*	
\$ESCAP	001514	8165#*	8546*	
\$ETABL	001546	8165#		
\$ETEND	001652	8165#		
\$FATAL	001530	7023*	8165#	
\$FFLG	000244	7023#*		
\$FILLC	001456	8165#	8546	
\$FILLS	001455	8165#	8546	
\$GDADR	001420	8165#		
\$GDDAT	001424	8165#		
\$GTSWR=	***** U	8546		
\$HIBTS	002136	8165#		
\$ICNT	001404	8165#	8546*	
\$INTAG	001435	8165#		
\$ITEMB	001414	8165#	8546*	
\$LF	001524	8165#	8546	
\$LFLG	000243	7023#*		
\$LPADR	001406	8165#*	8546*	
\$LPERR	001410	8165#*	8546*	
\$MADR1	001560	8165#		
\$MADR2	001564	8165#		
\$MADR3	001570	8165#		
\$MADR4	001574	8165#		
\$MAIL	001526	8165#	8546	
\$MAMS1	001556	8165#		
\$MAMS2	001562	8165#		
\$MAMS3	001566	8165#		
\$MAMS4	001572	8165#		
\$MBADR	002140	8165#		
\$MFLG	000242	7023#*		
\$MSGAD	001542	7023*	8165#	
\$MSGLG	001544	7023*	8165#	
\$MSGTY	001526	7023*	8165#	
\$MTYP1	001557	8165#		
\$MTYP2	001563	8165#		
\$MTYP3	001567	8165#		
\$MTYP4	001573	8165#		
\$MXCNT	016624	8546#		

